

CHELSEA DJ2 CP UMA Schematics Document

Arrandale

Intel PCH

2010-05-18

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REV : A00

DY : Nopop Component

HDMI : Pop for HDMI function

GIGA : Pop for GIGA LAN

10/100 : Pop for 10/100 LAN

65 BOM : Nopop for 65 BOM option

for 65 BOM



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Title

Cover Page

Size
A3

Document Number

DJ2 CP UMA

Rev

A00

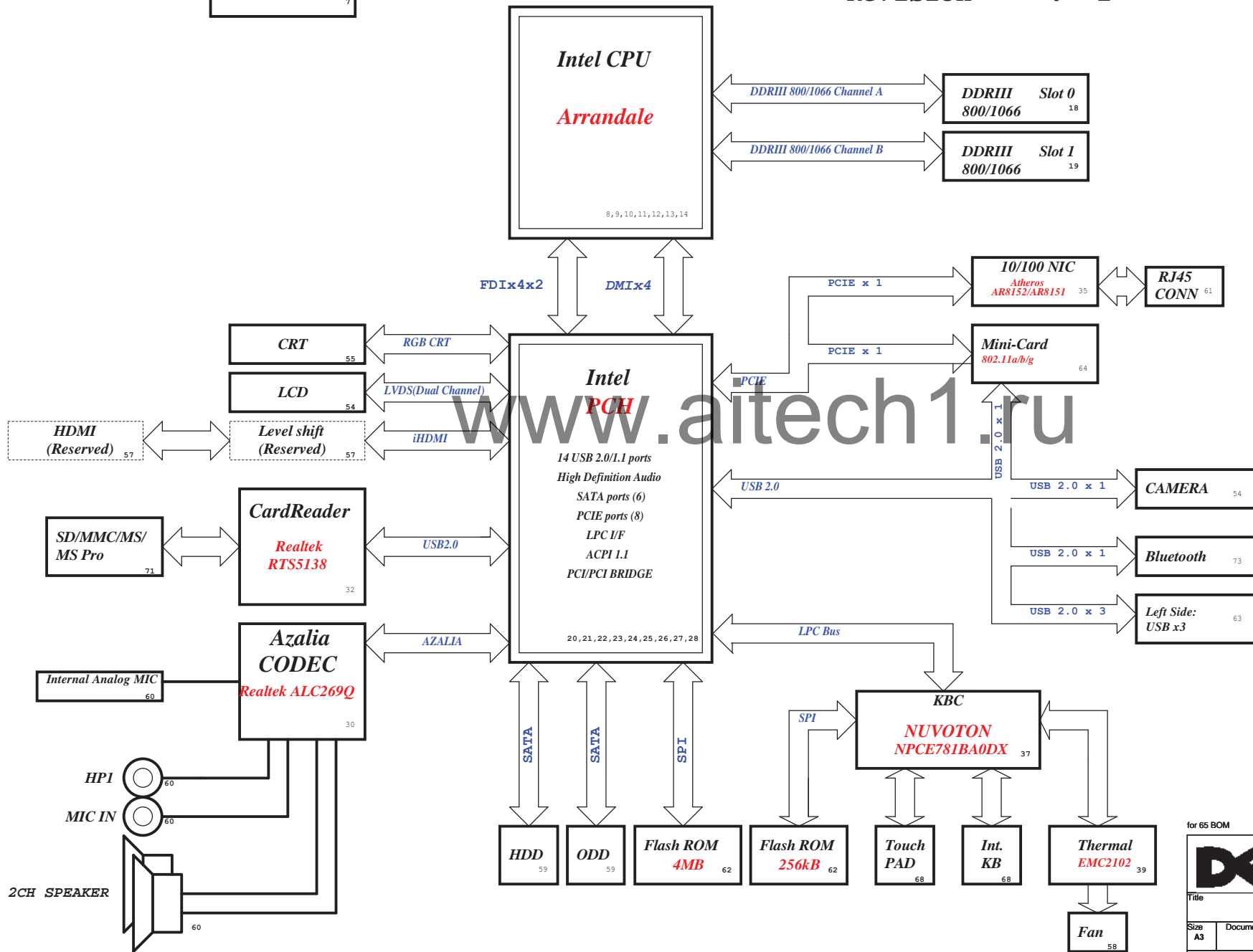
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CHELSEA DJ2 CP UMA Block Diagram

Project code : 91.4EM01.001
PCB P/N : 48.4EM17.011
Revision : -1

Clock Generator
SLG8SP585

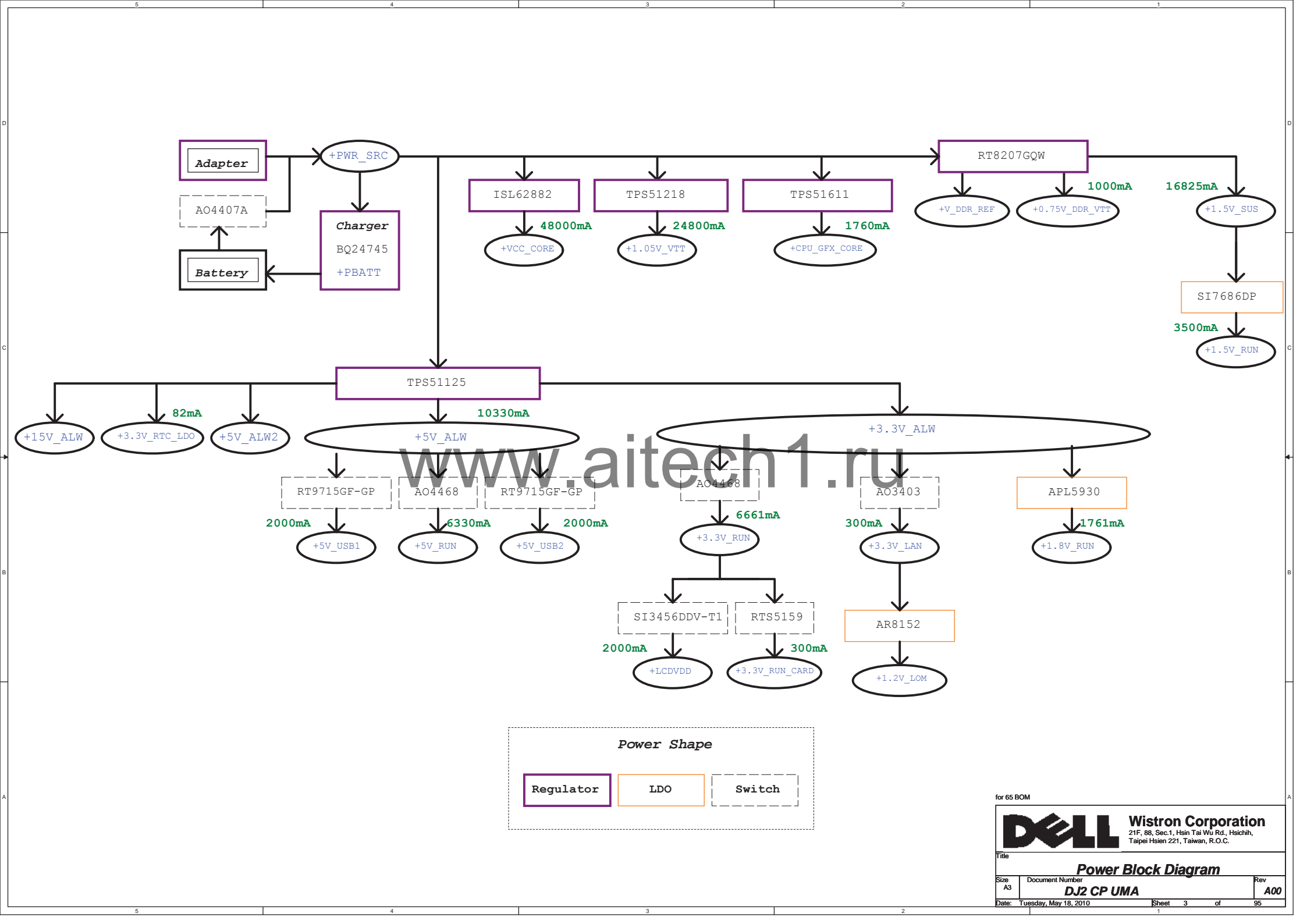


CPU DC/DC ISL62882	
INPUTS	
+PWR_SRC	
SYSTEM DC/DC TPS51218	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT
SYSTEM DC/DC RT8205BGQW 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC RT8207GQW 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC APL5930KAI 90	
INPUTS	OUTPUTS
+1.5V_SUS	+1.1V_RUN
VGA RT8208BGQW 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE
MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_DELAY
SYSTEM DC/DC Switches 42	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top L2: GND L3: Signal L4: Signal L5: VCC L6: Bottom	

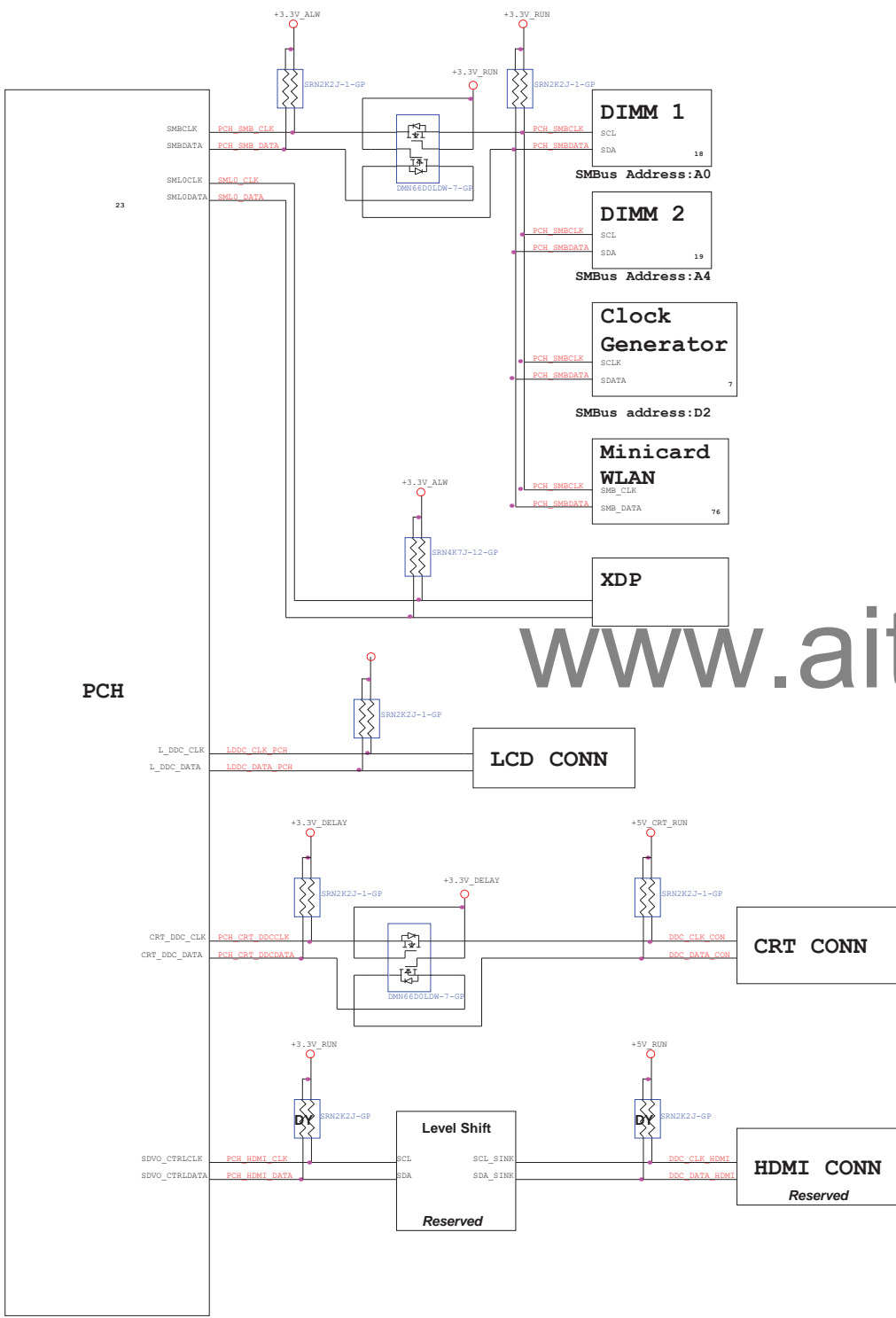
for 6S BOM

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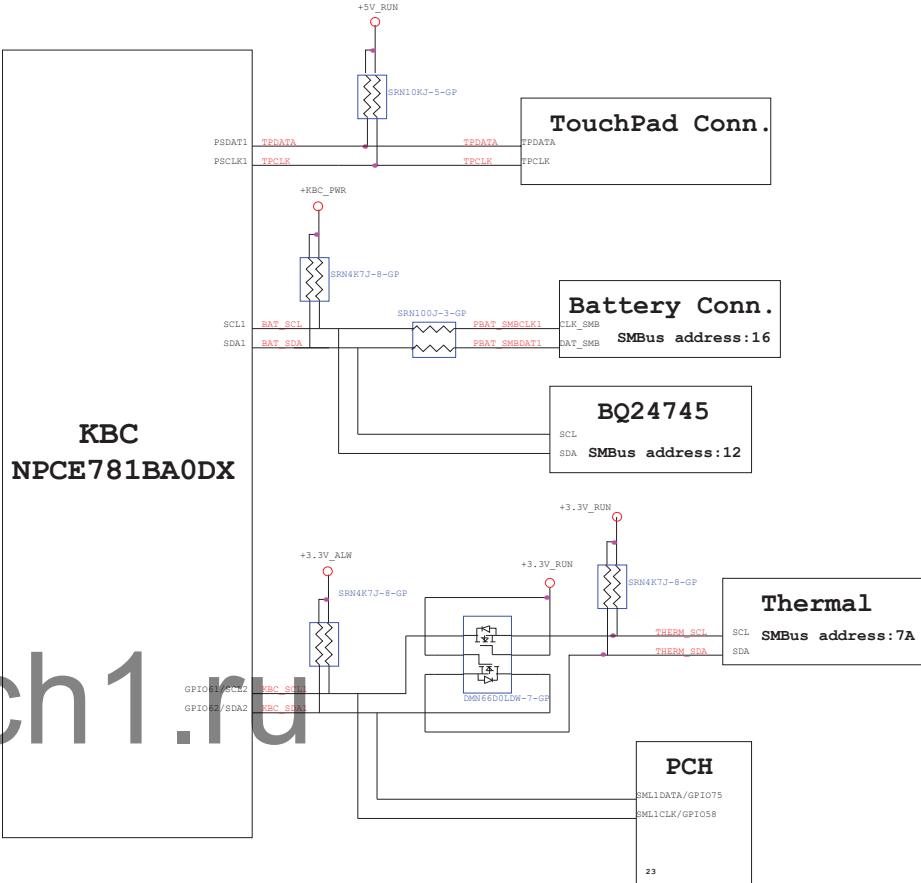
Title Block Diagram	
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PCH SMBus Block Diagram

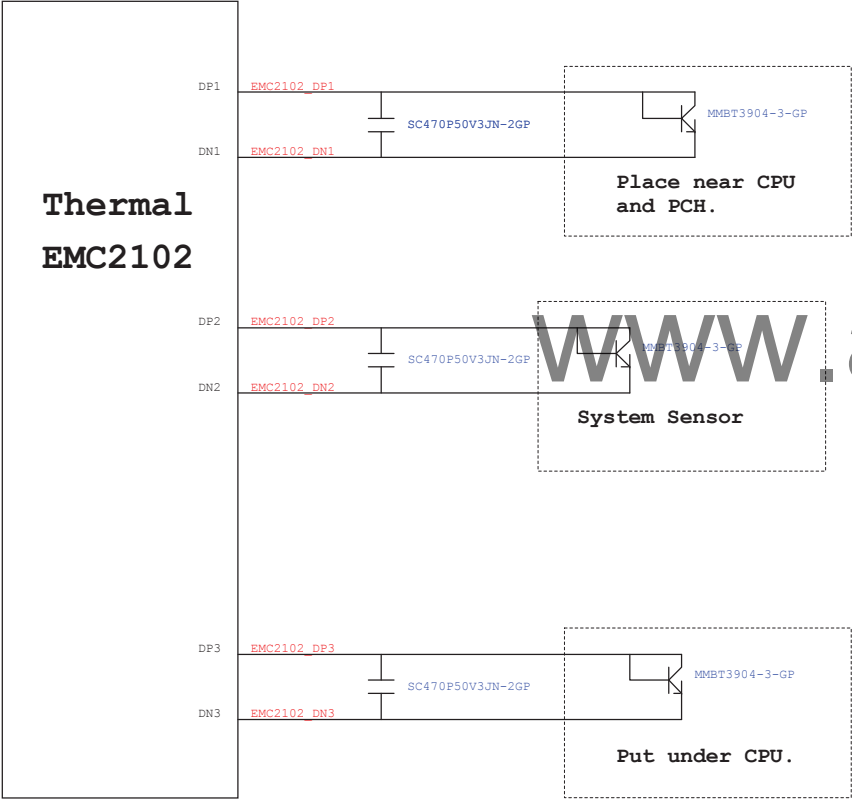


KBC SMBus Block Diagram

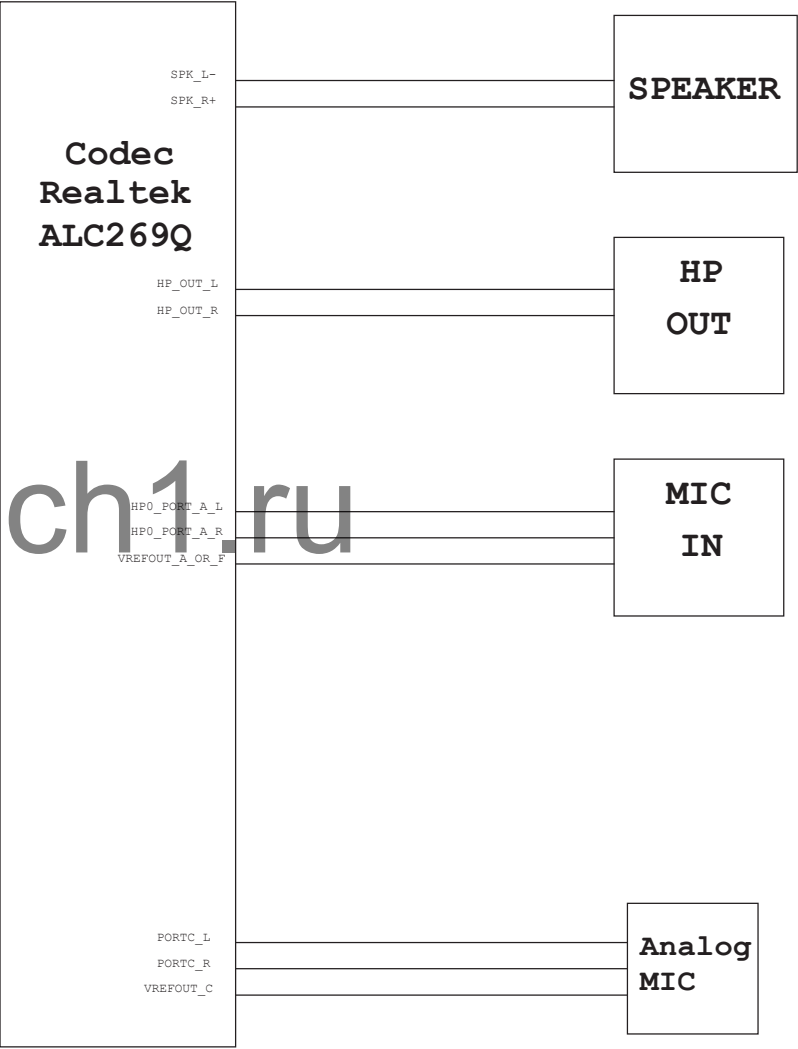


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Thermal Block Diagram



Audio Block Diagram



PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table


USB	
Pair	Device
0	USB0
1	X
2	USB2
3	USB3
4	X
5	WLAN
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

Processor Strapping

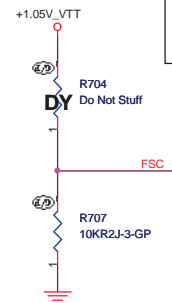
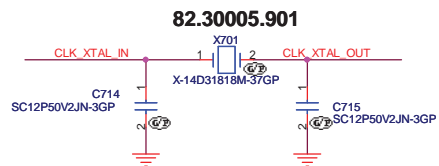
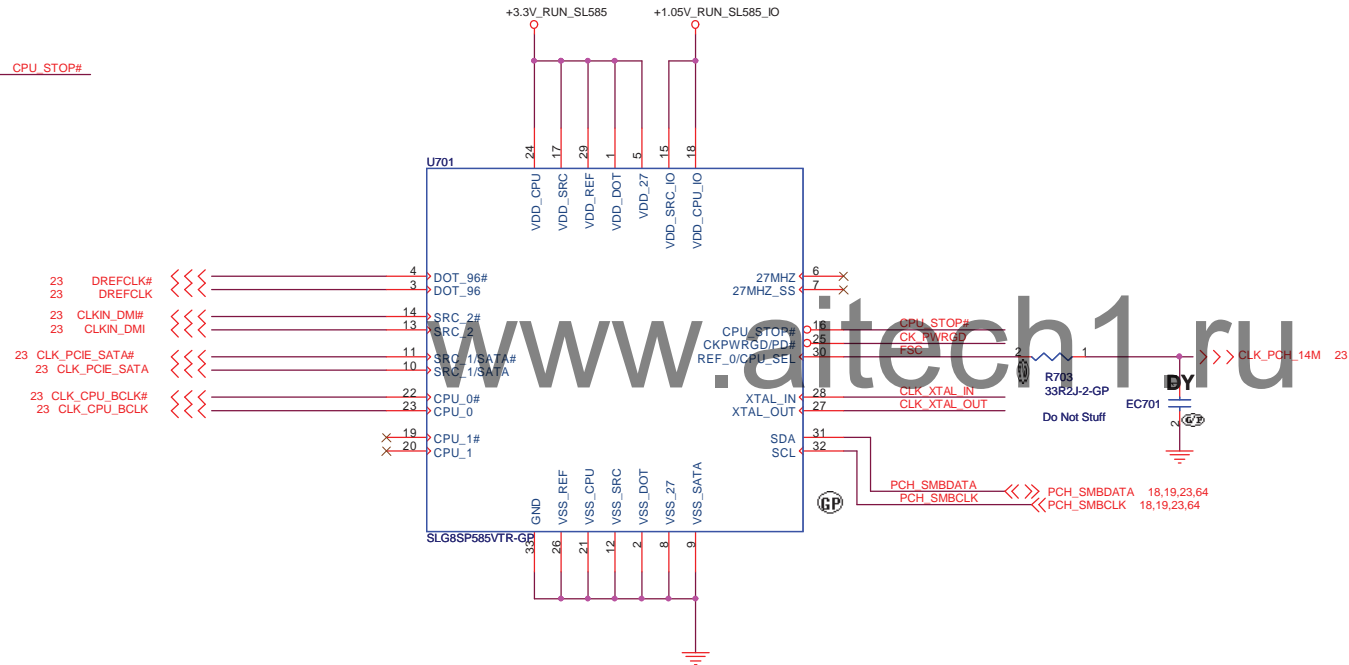
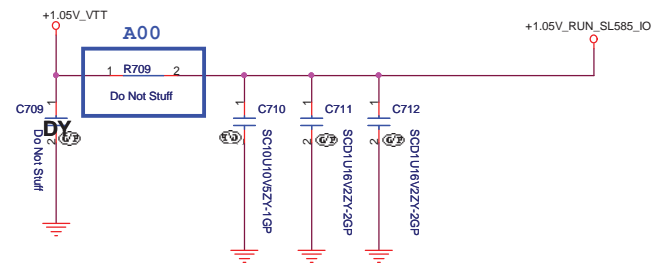
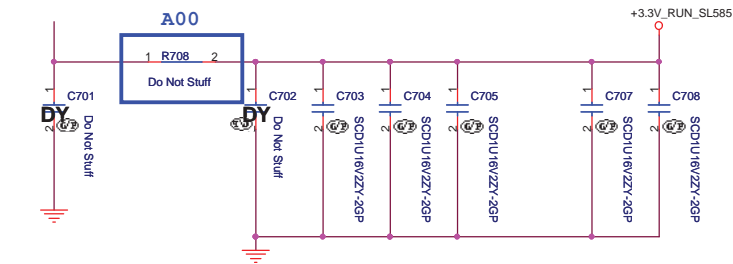
Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

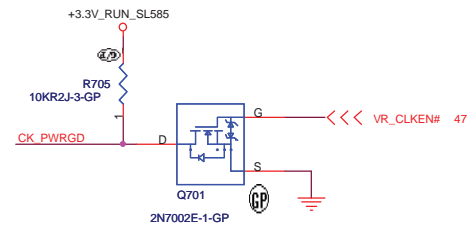
for 65 BOM

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SSID = CLOCK



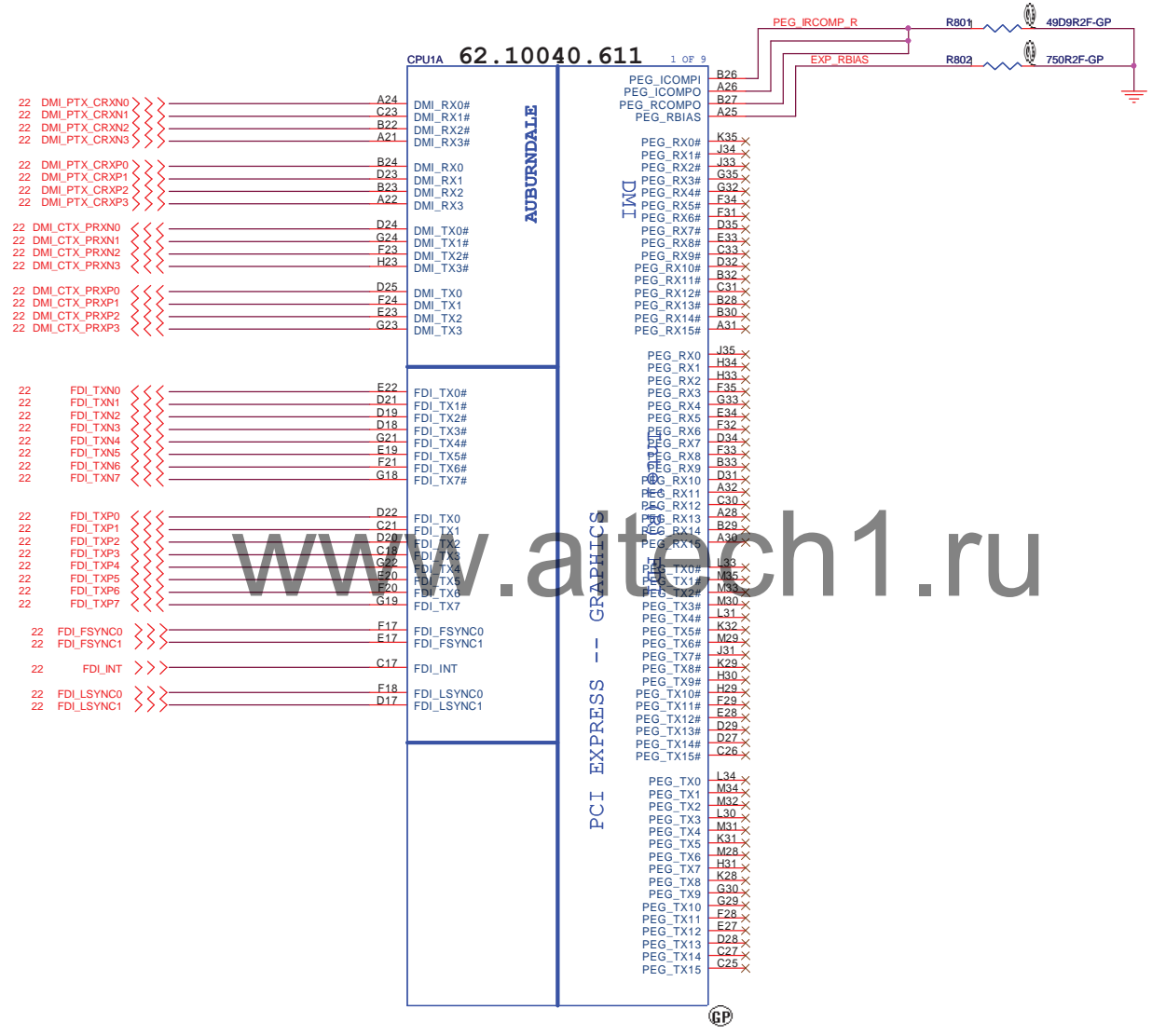
FSC	0	1
SPEED	133MHz (Default)	100MHz

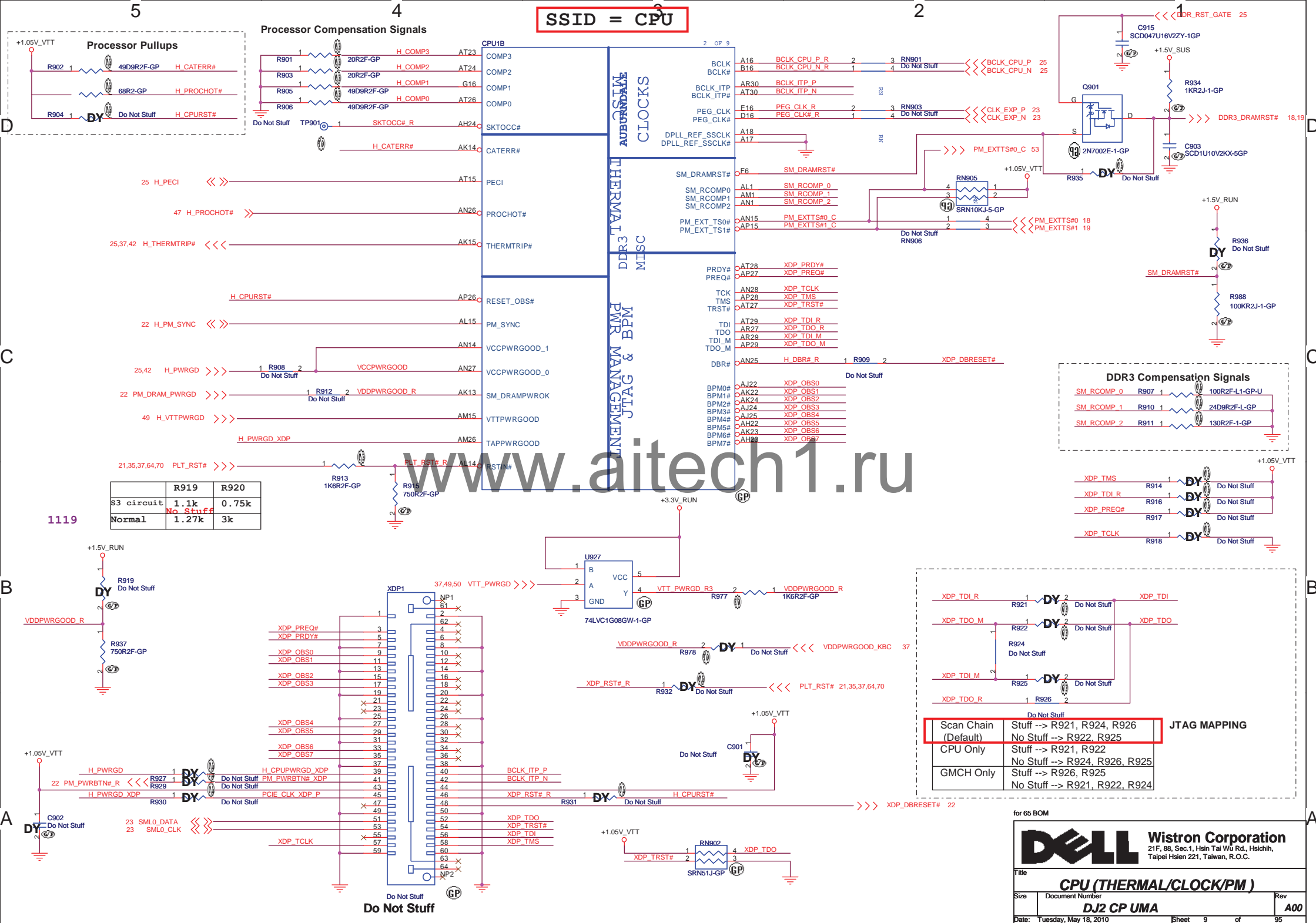


for 65 BOM

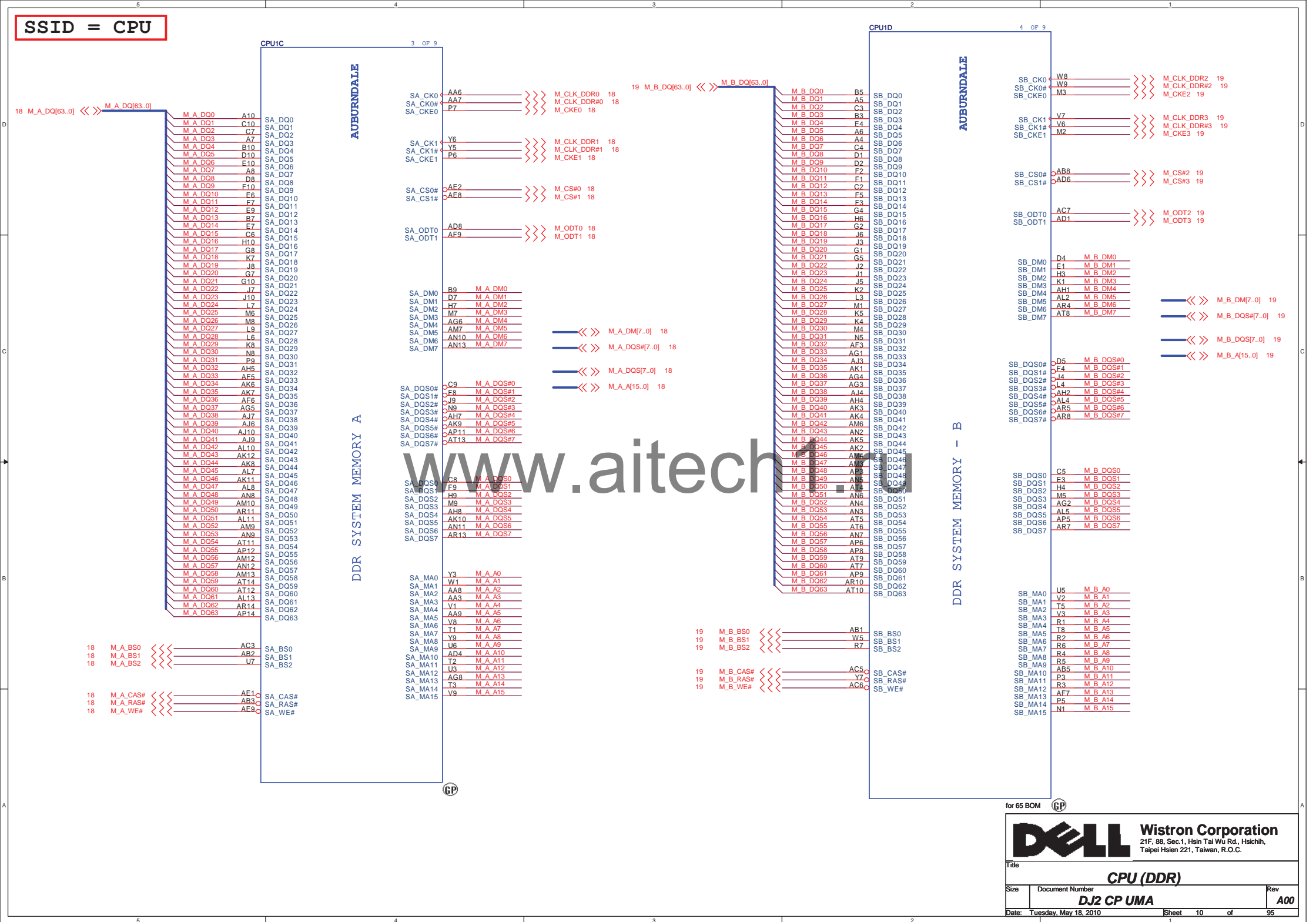


SSID = CPU





SSID = CPU

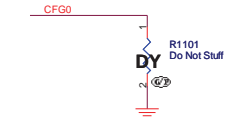


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Title: **CPU (DDR)**
Size: Document Number: **DJ2 CP UMA** Rev: **A00**
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SSID = CPU

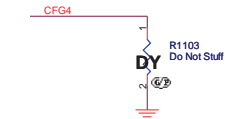


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

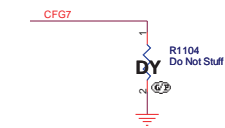


CFG3 - PCI-Express Static Lane Reversal	
CFG3	1:Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

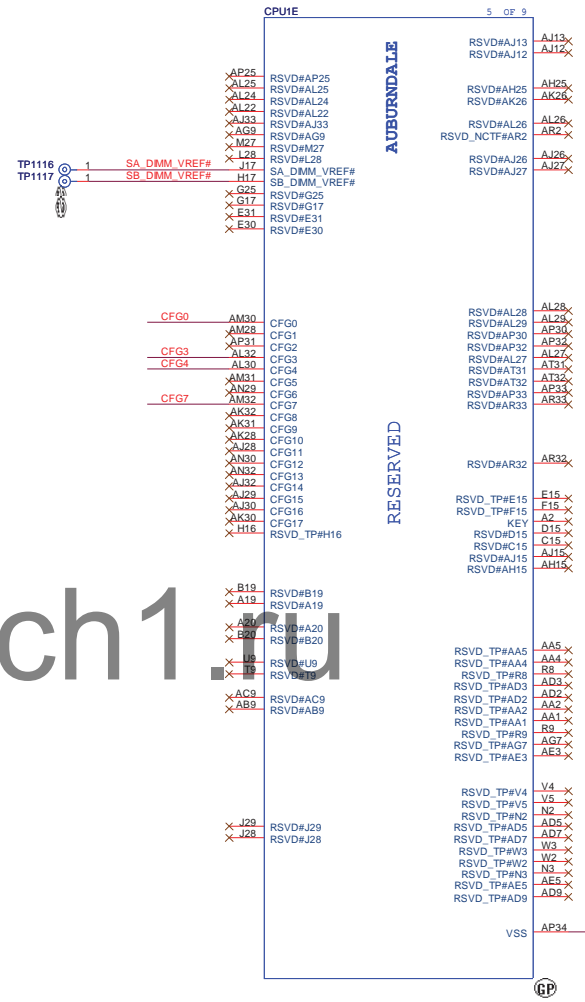
Change to Normal operation
20100202



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

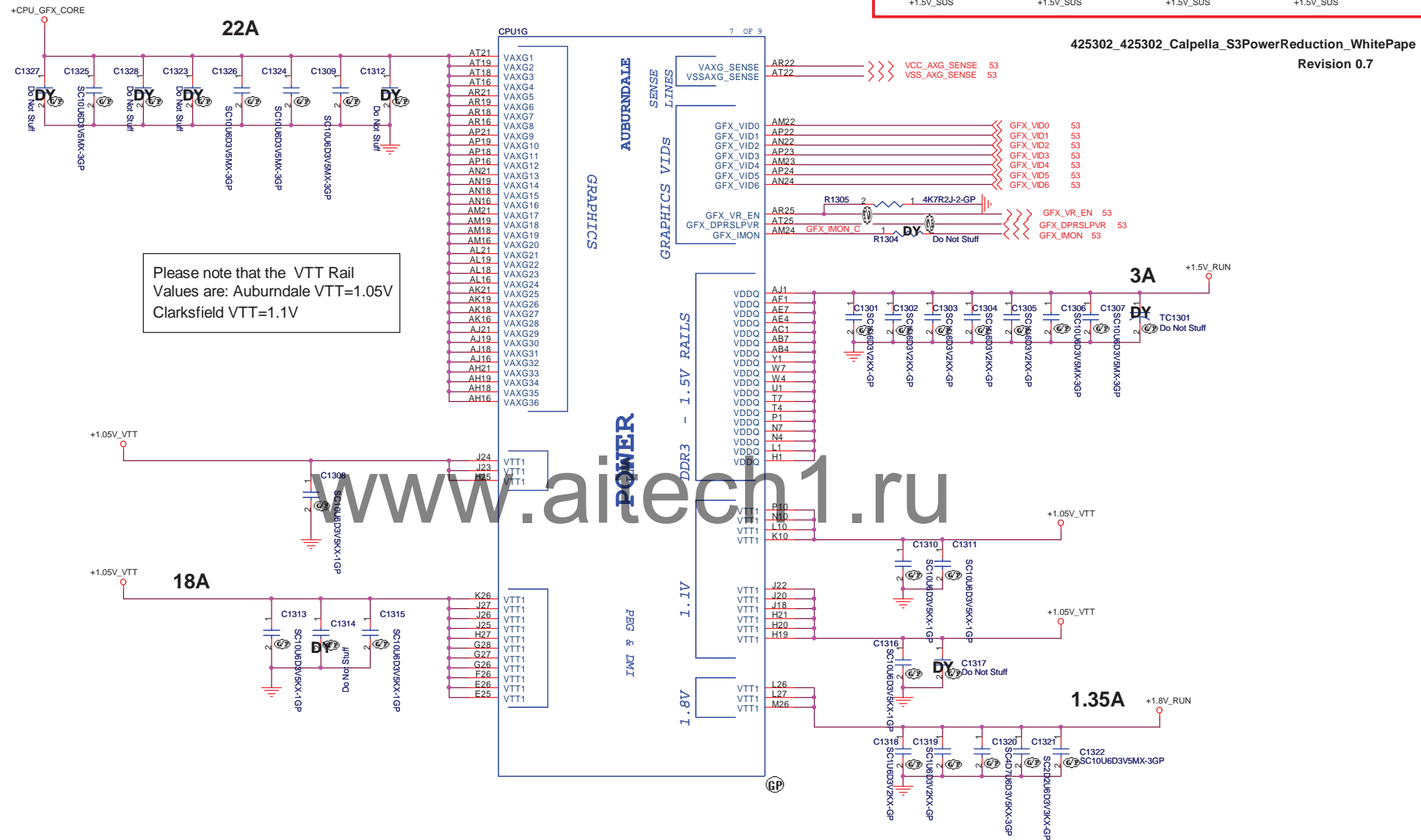


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is
CRB implementation; EDS/DG
recommendation to GND.

SSID = CPU



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CPU (VCC GFXCORE)

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DJ2 CP UMA

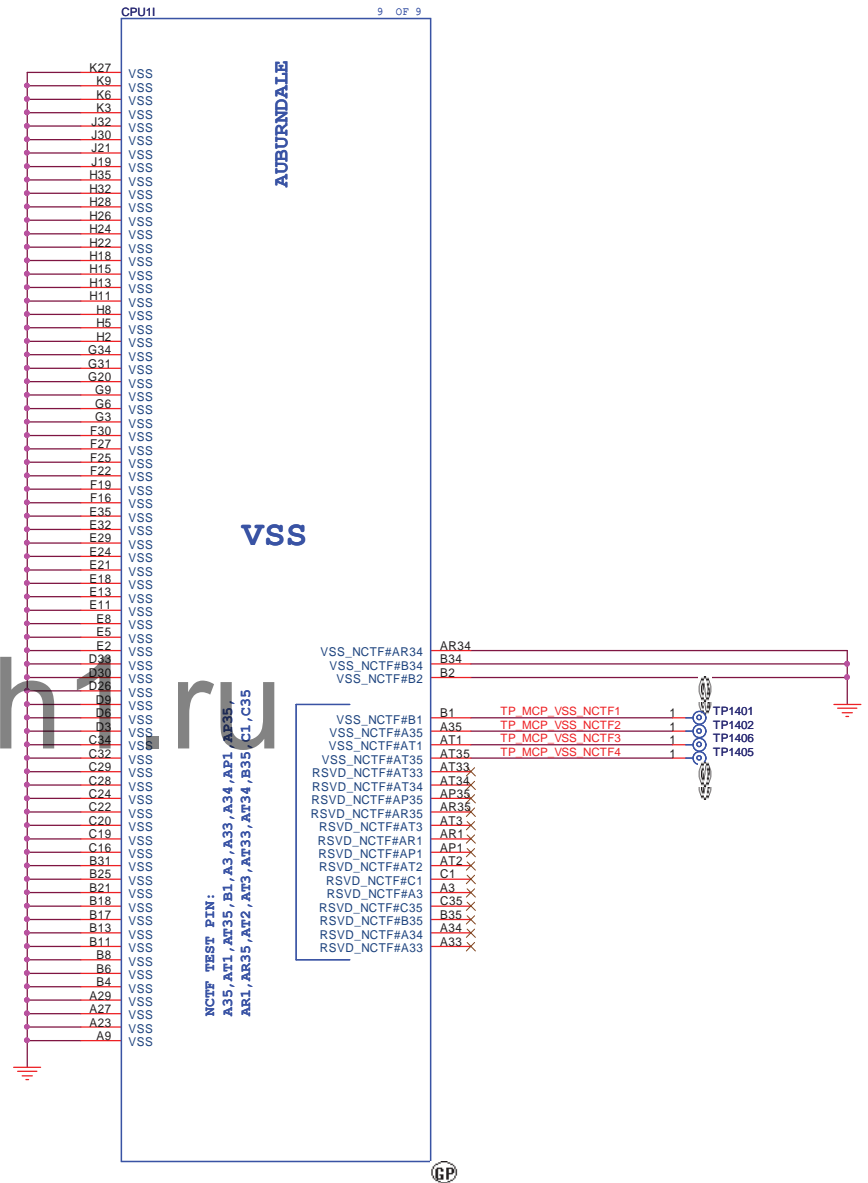
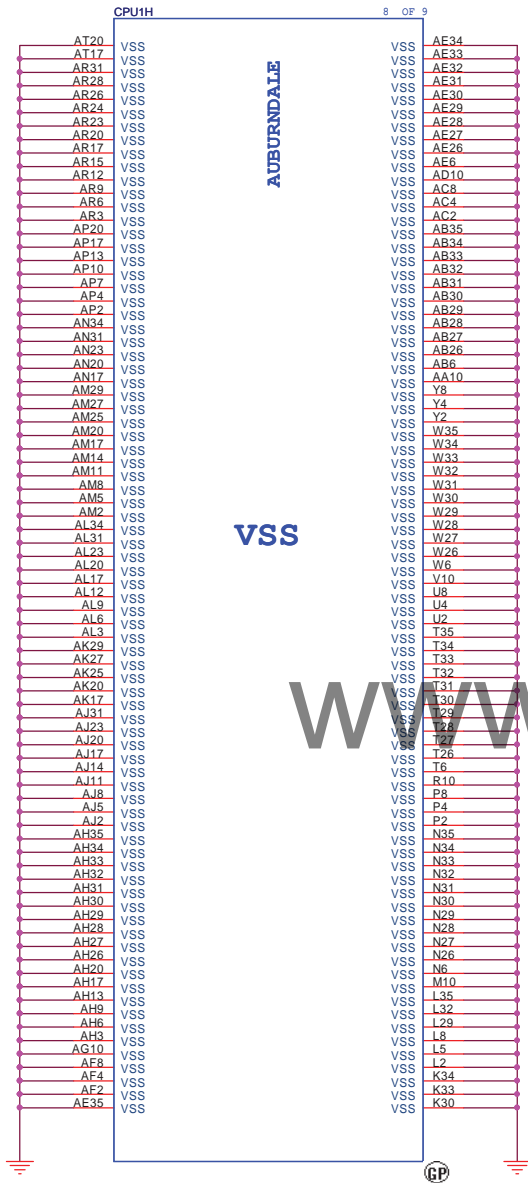
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SSID = CPU



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CPU (VSS)

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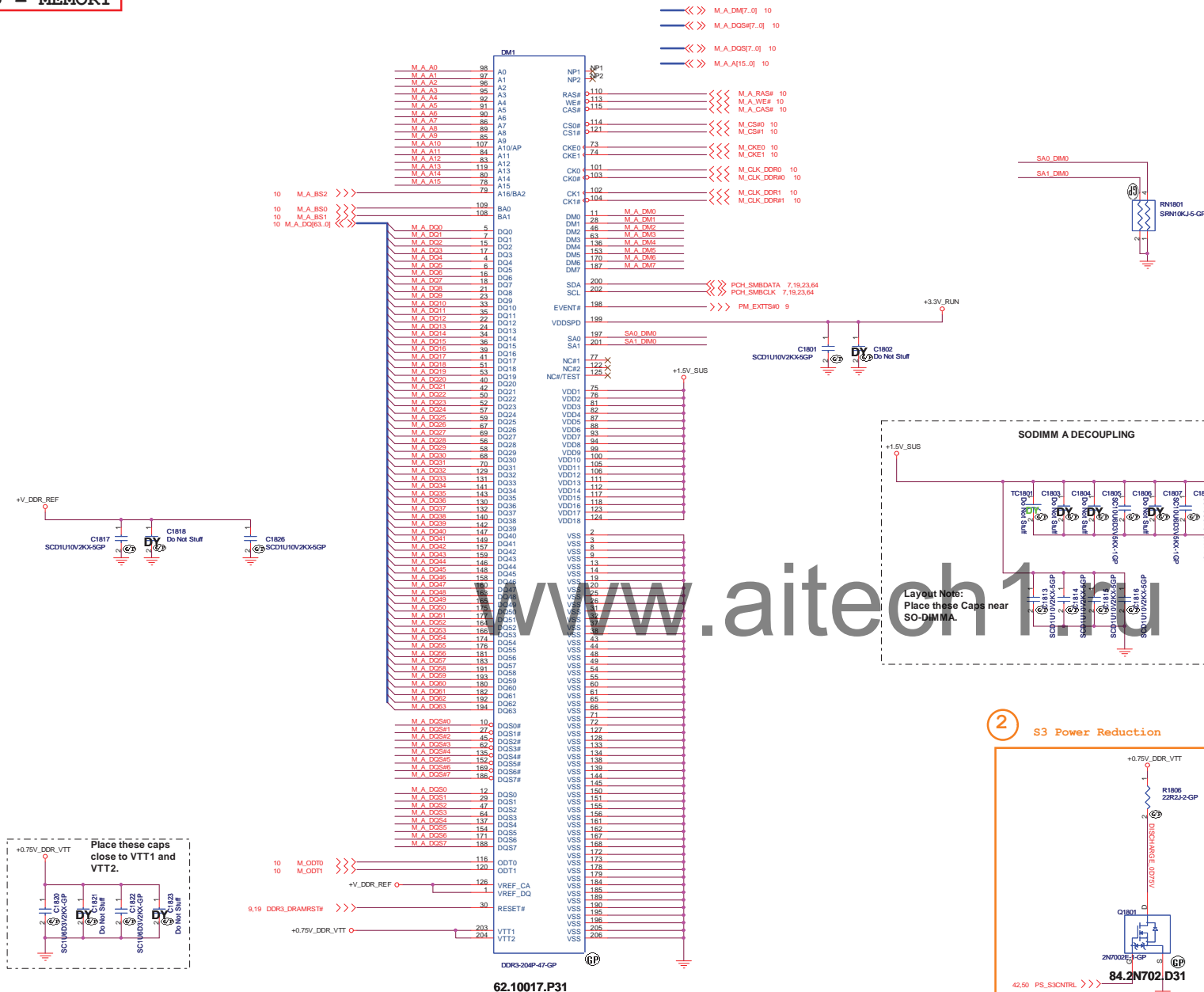
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Reserved

SSID = MEMORY



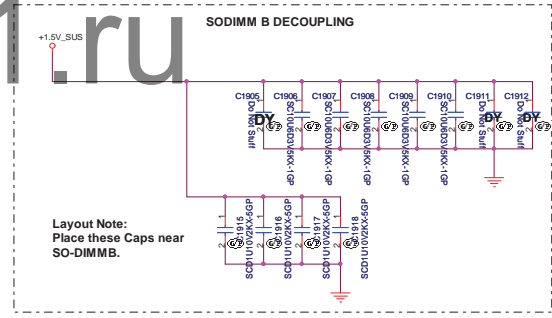
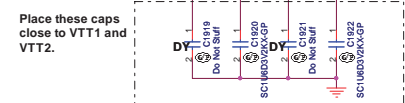
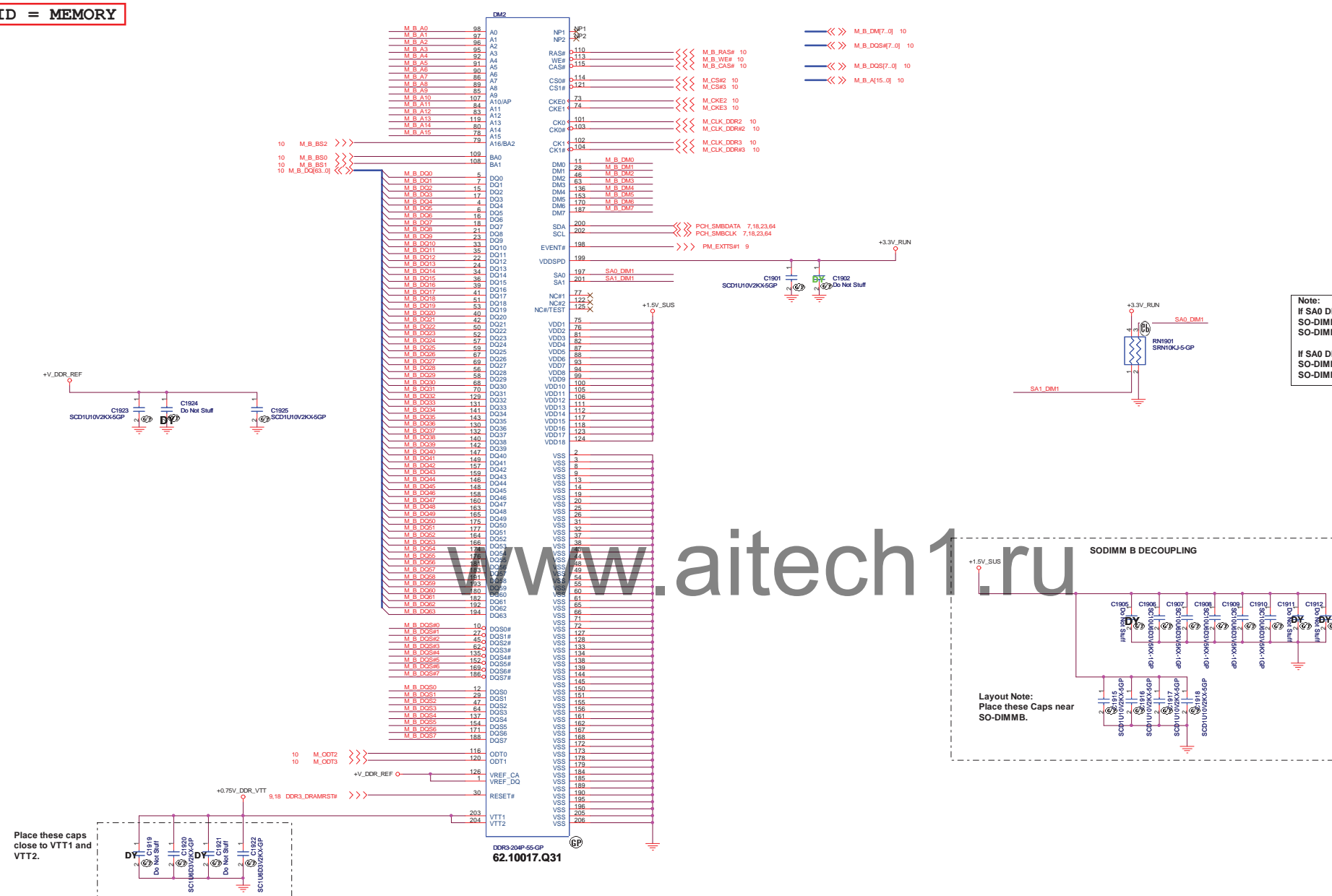
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Layout Note:
Place these Caps near
SO-DIMMA.

② S3 Power Reduction

SSID = MEMORY



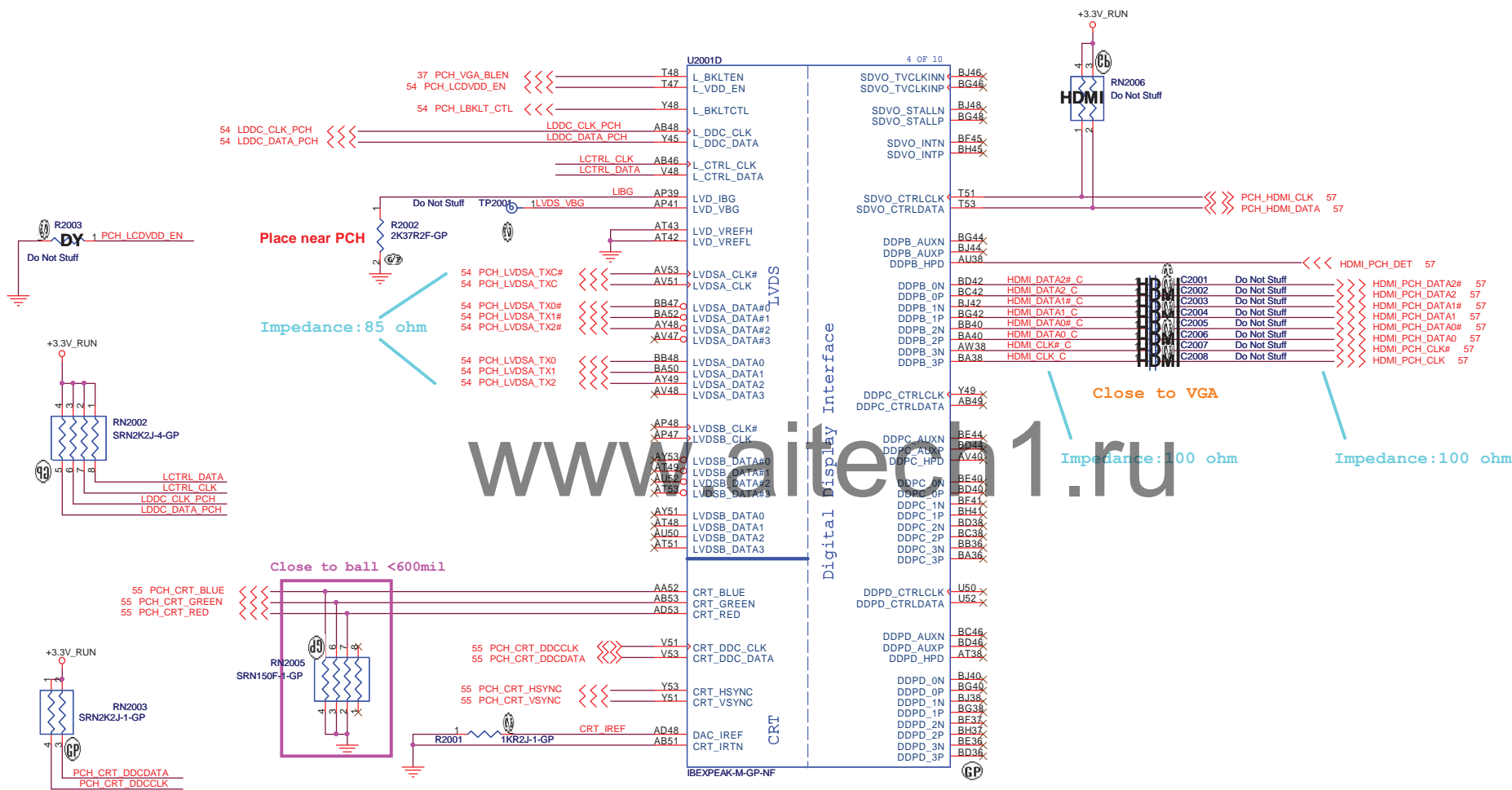
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

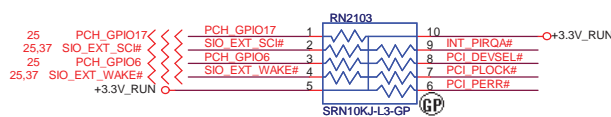
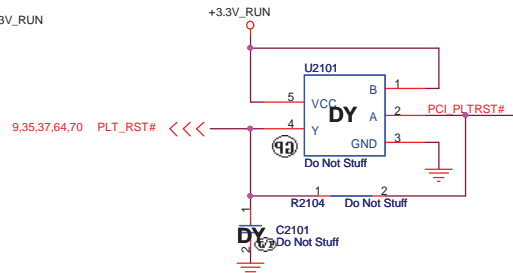
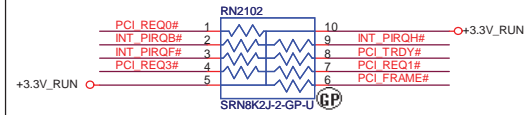
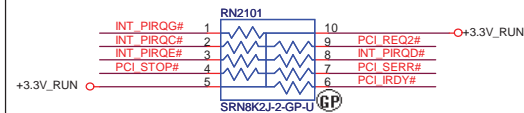
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from
the Processor than SO-DIMMA

SSID = PCH

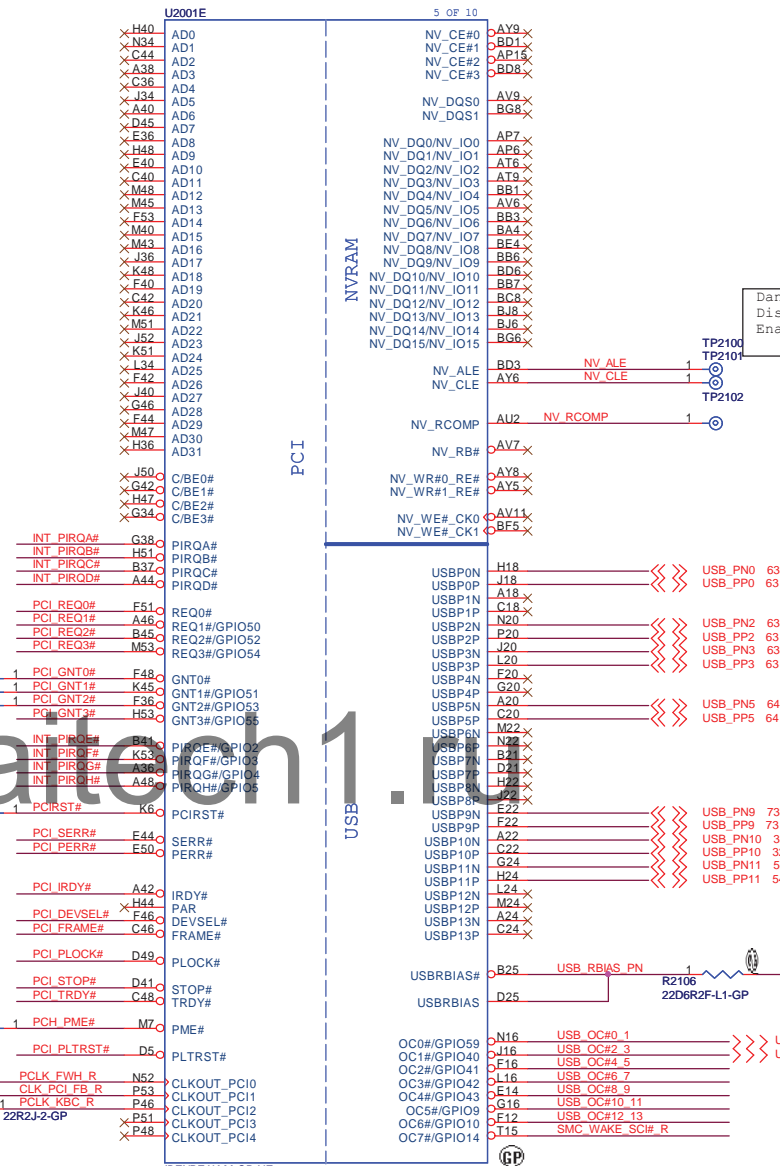
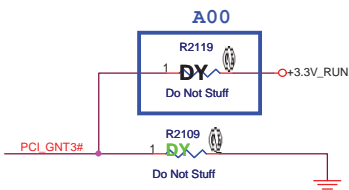


SSID = PCH

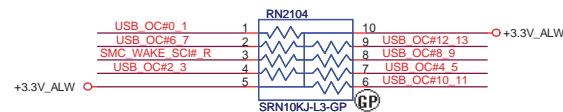


BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



USB	
Pair	Device
0	USB0
1	X
2	USB2
3	USB3
4	X
5	WLAN
6	X
7	X
8	X
9	BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X



for 65 BOM



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PCH (PCI/USB/NVRAM)

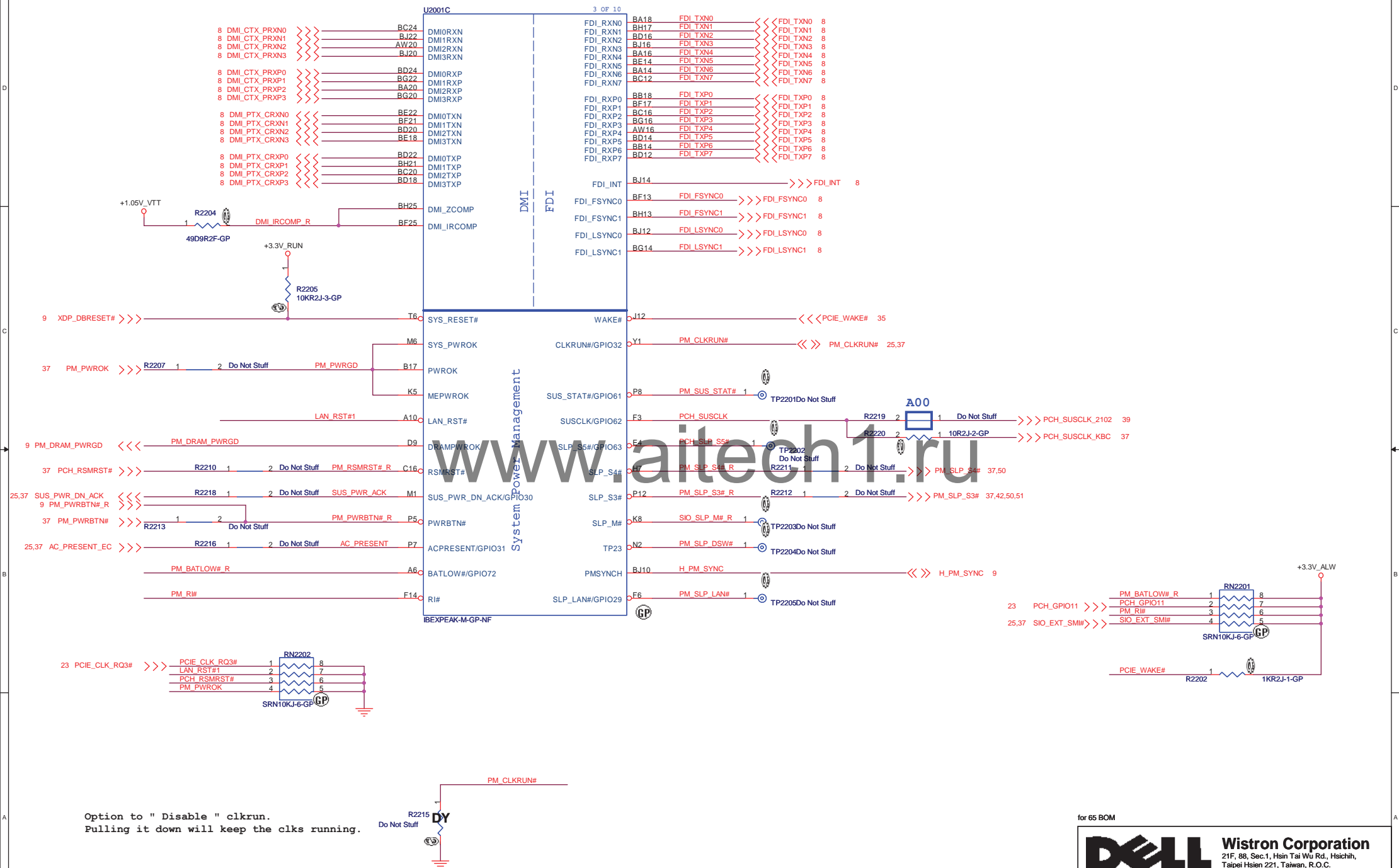
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SSID = PCH



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PCH (DM I/FDI/PM)

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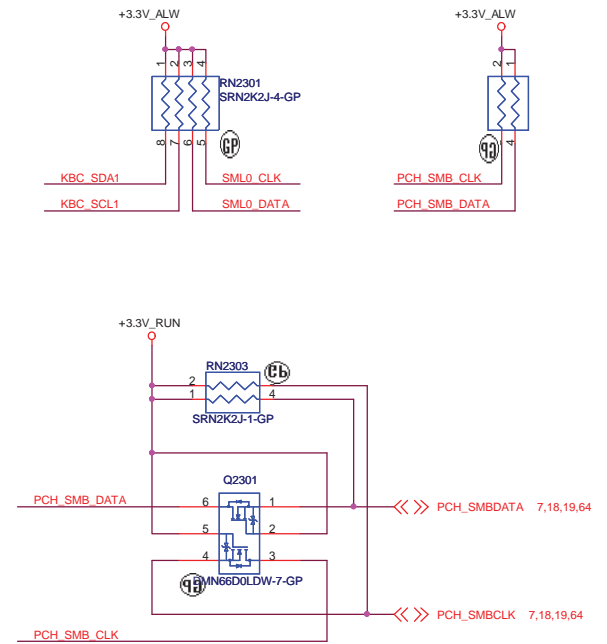
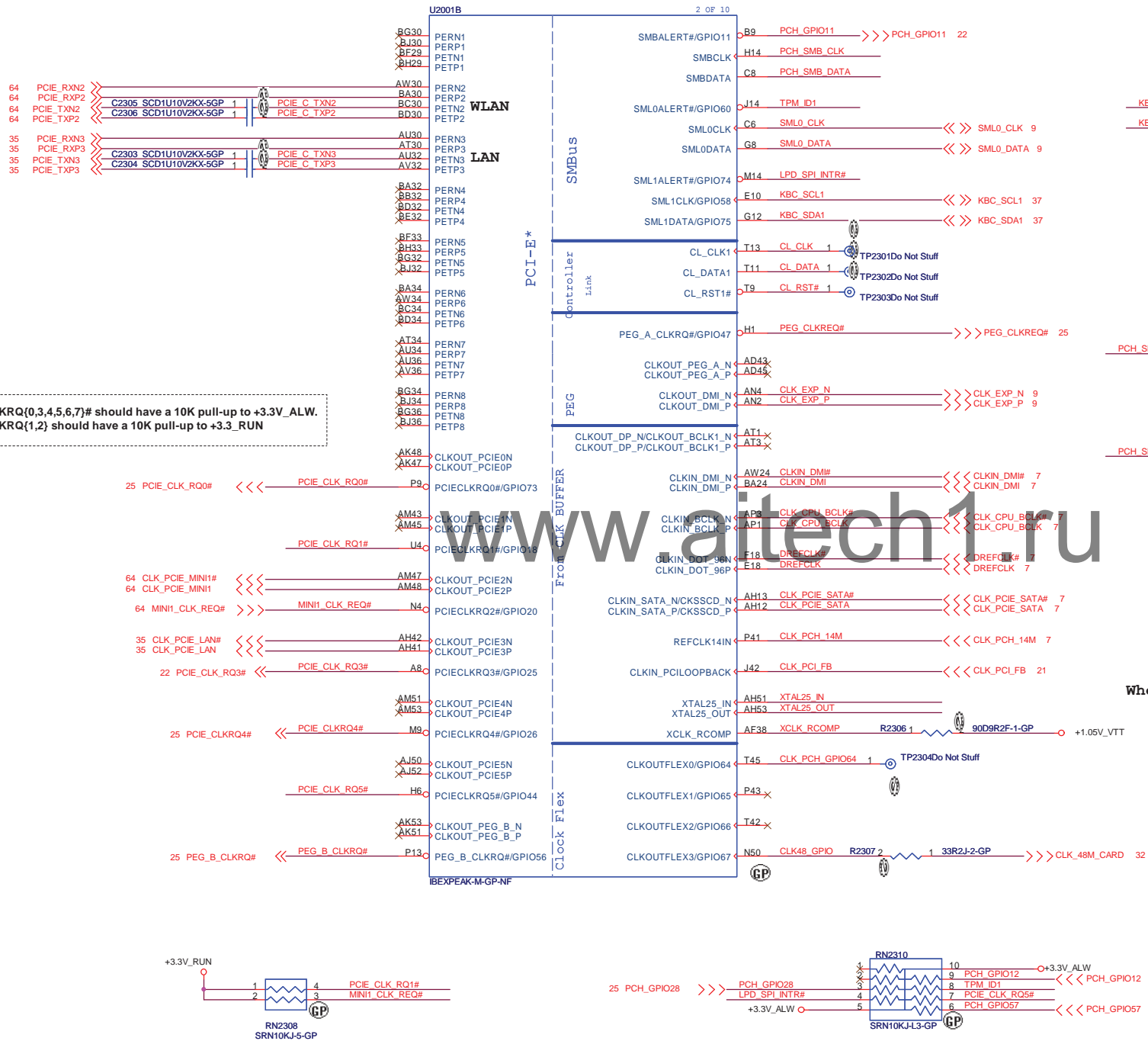
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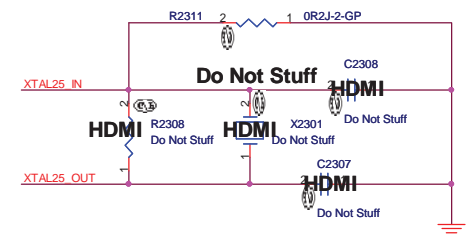
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SSID = PCH



Need DY when HDMI pop
When HDMI parts stuffed, the R2311 need DY.

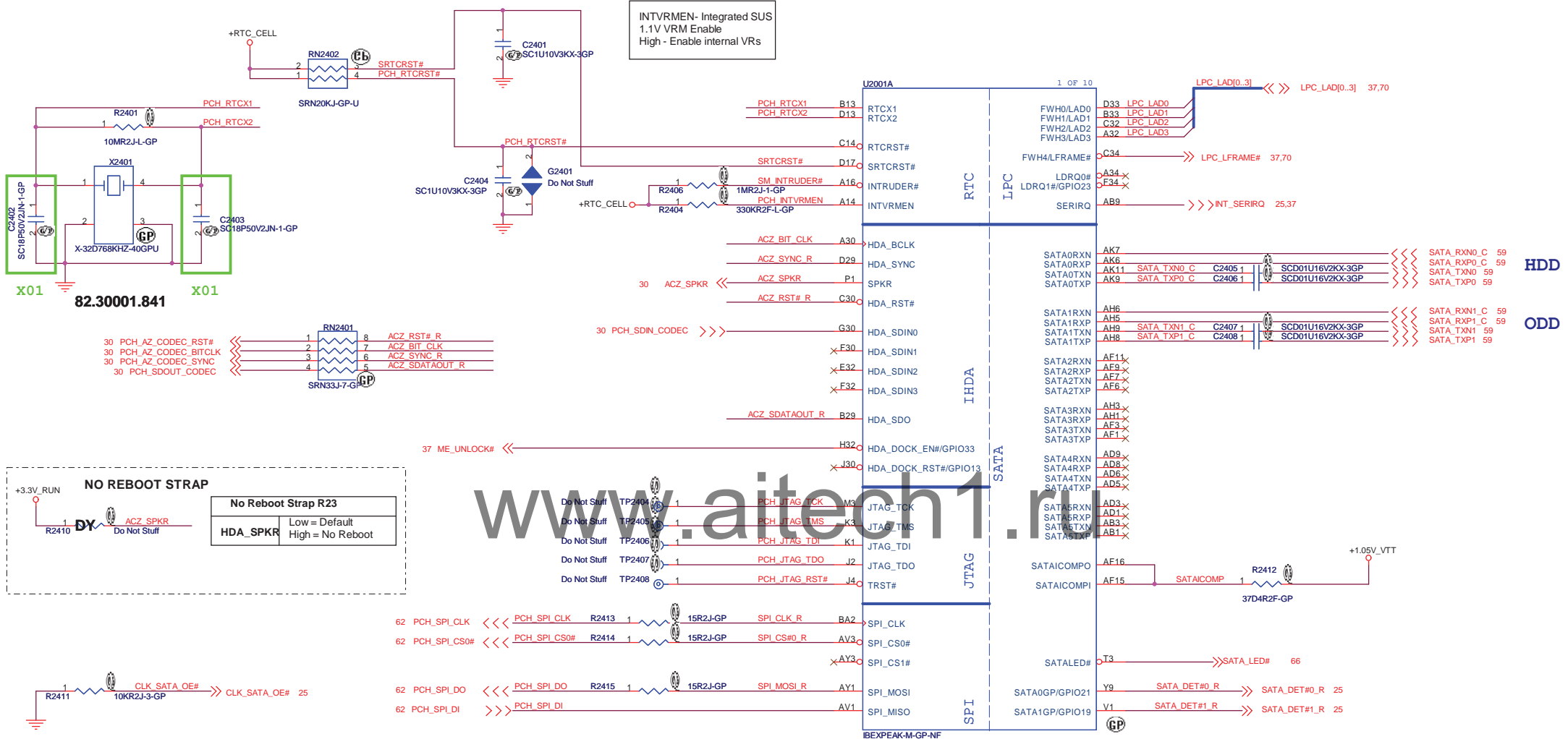


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Title **PCH (PCI-E/SMBUS/CLOCK/CL)**
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SSID = PCH



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PCH (SPI/RTC/LPC/SATA/IHDA)

Size

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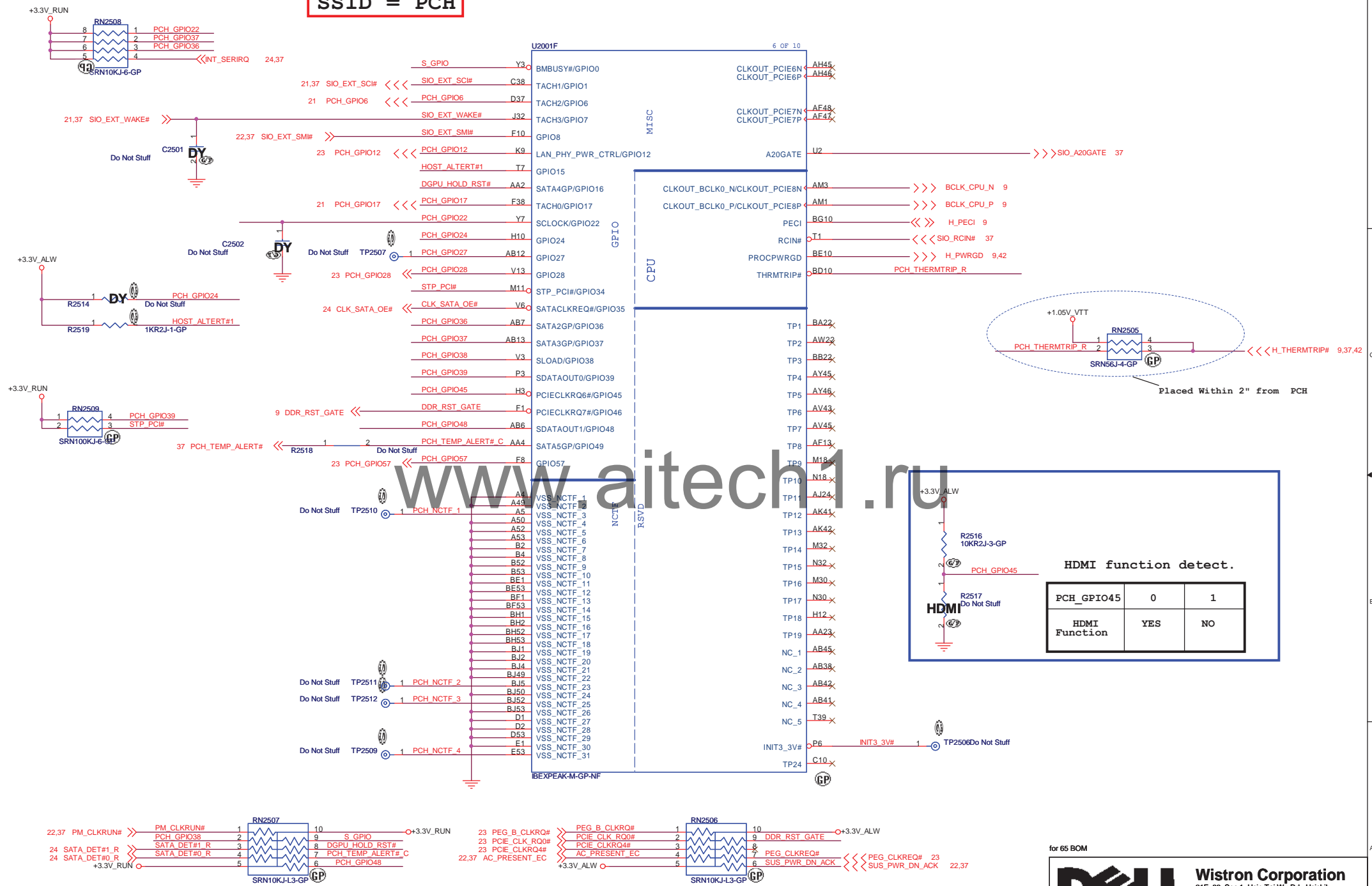
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SSID = PCH



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PCH (GPIO/CPU)

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Document Number

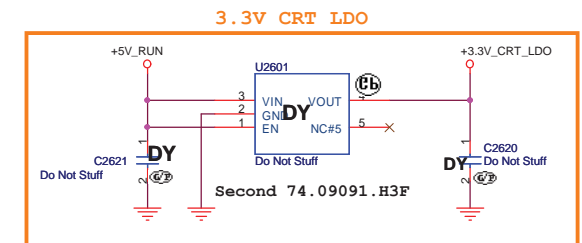
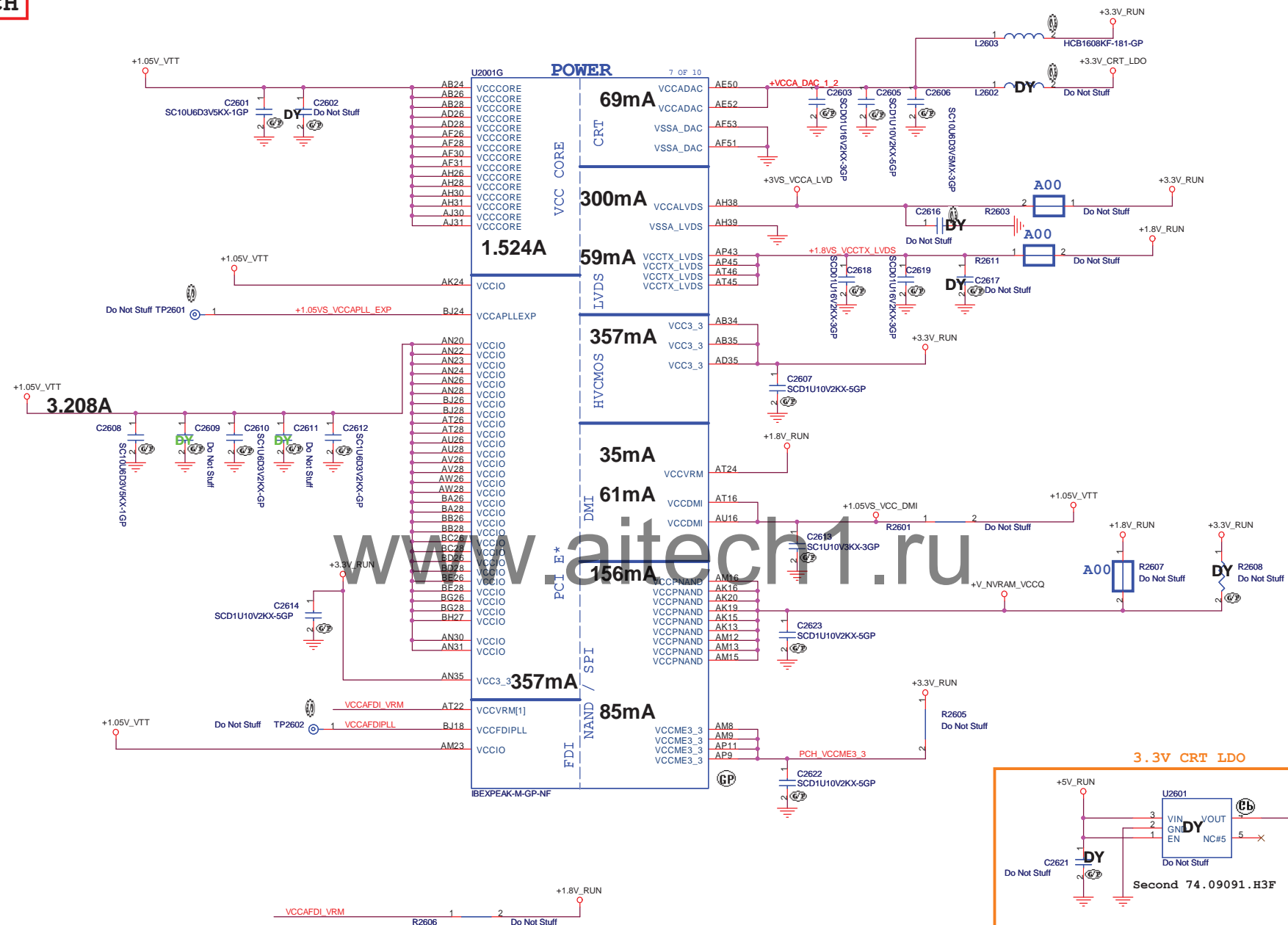
DJ2 CP UMA

Date: Tuesday, May 18, 2010

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A00

SSID = PCH



for 65 BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (POWER1)

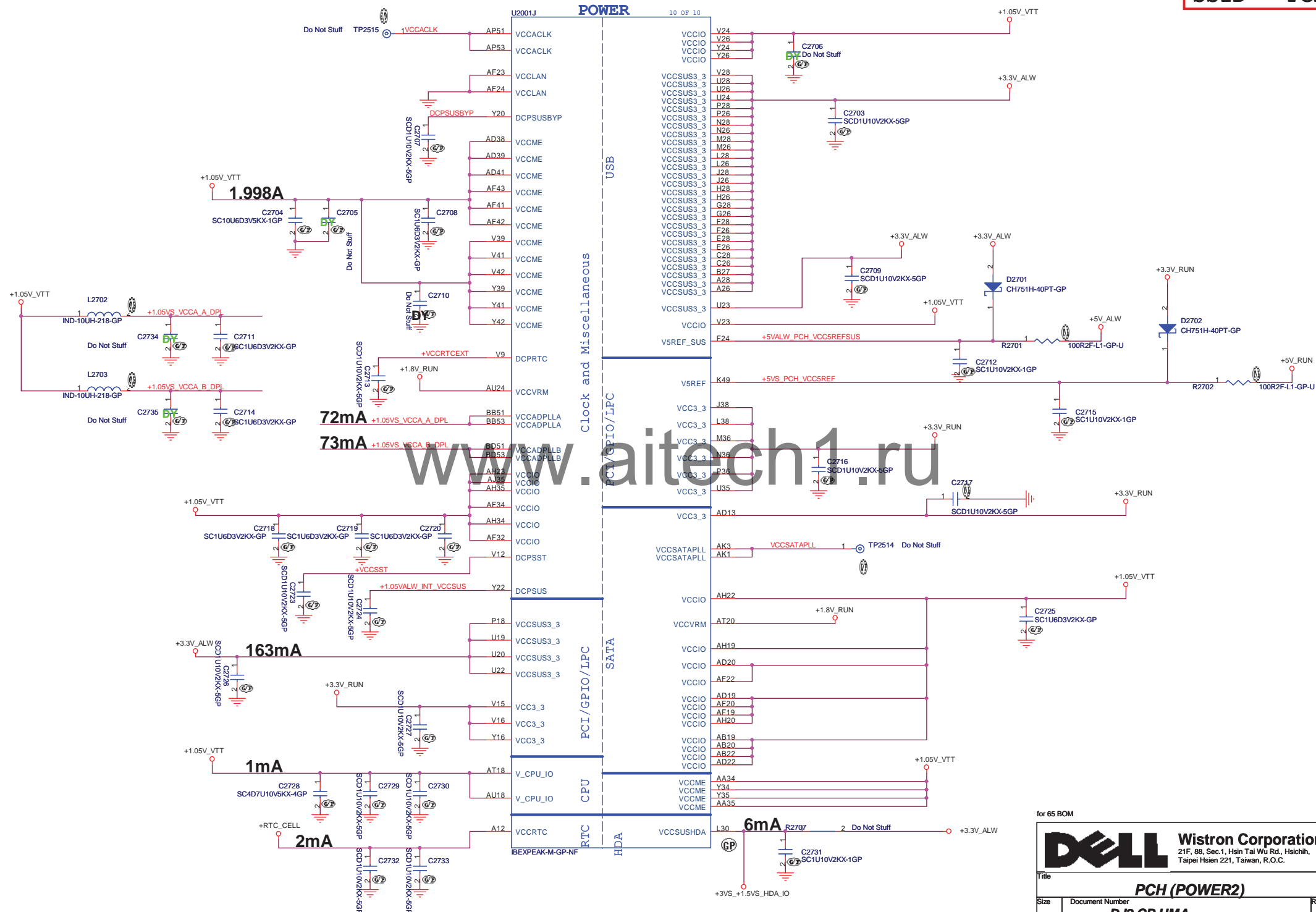
Size	Document Number
------	-----------------

DJ2 CP UMA

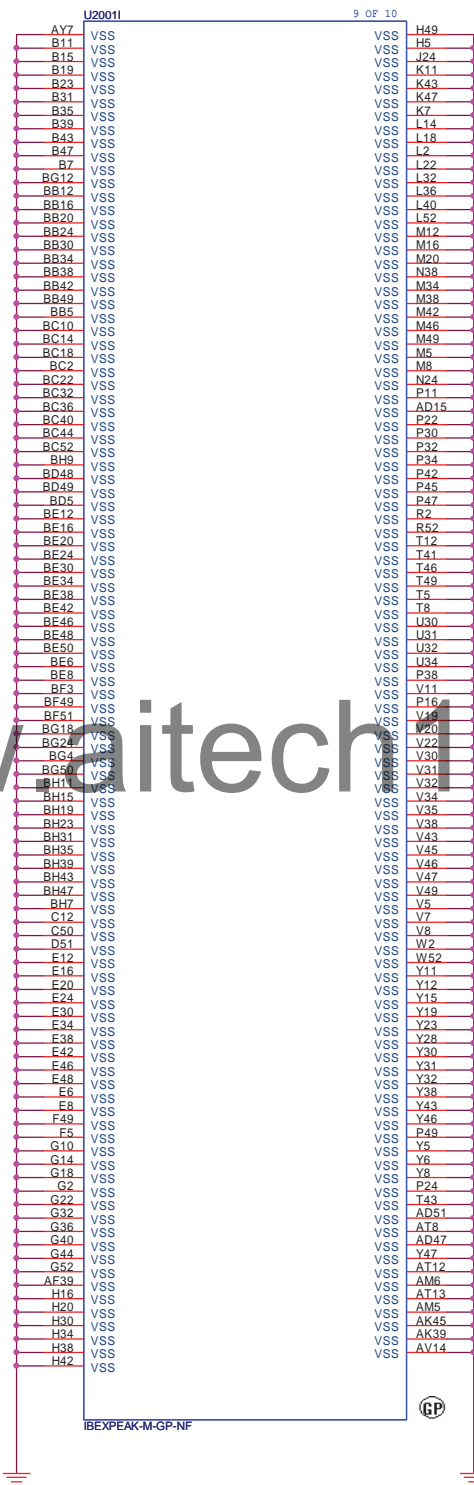
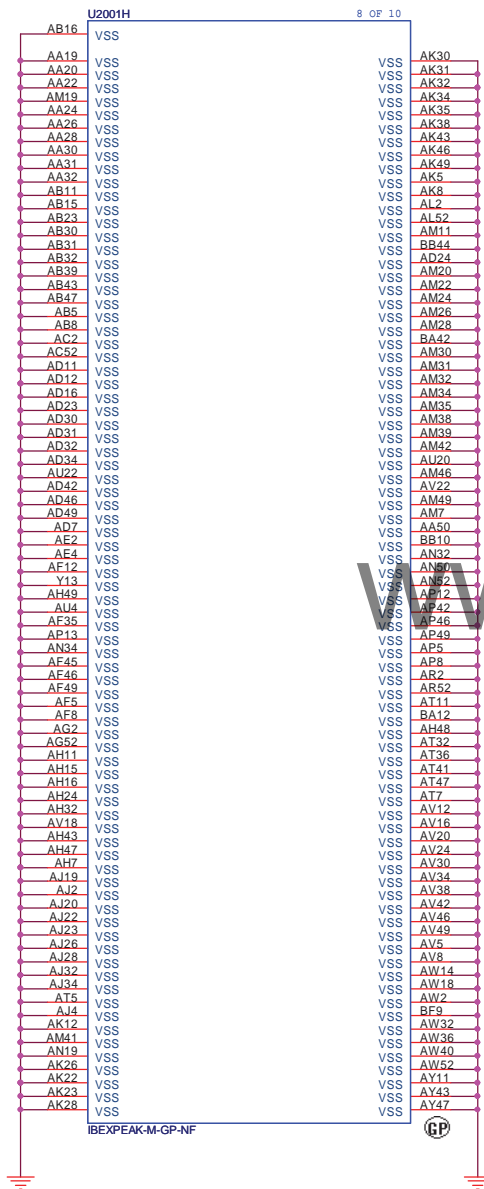
Date: Tuesday, May 18, 2010

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Product	20	50	80
1			



SSID = PCH



for 65 BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
Title																													

PCH (VSS)

Size	Document Number
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A00


Date: Tuesday, May 18, 2010

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for 65 BOM



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
DJ2 CP UMA

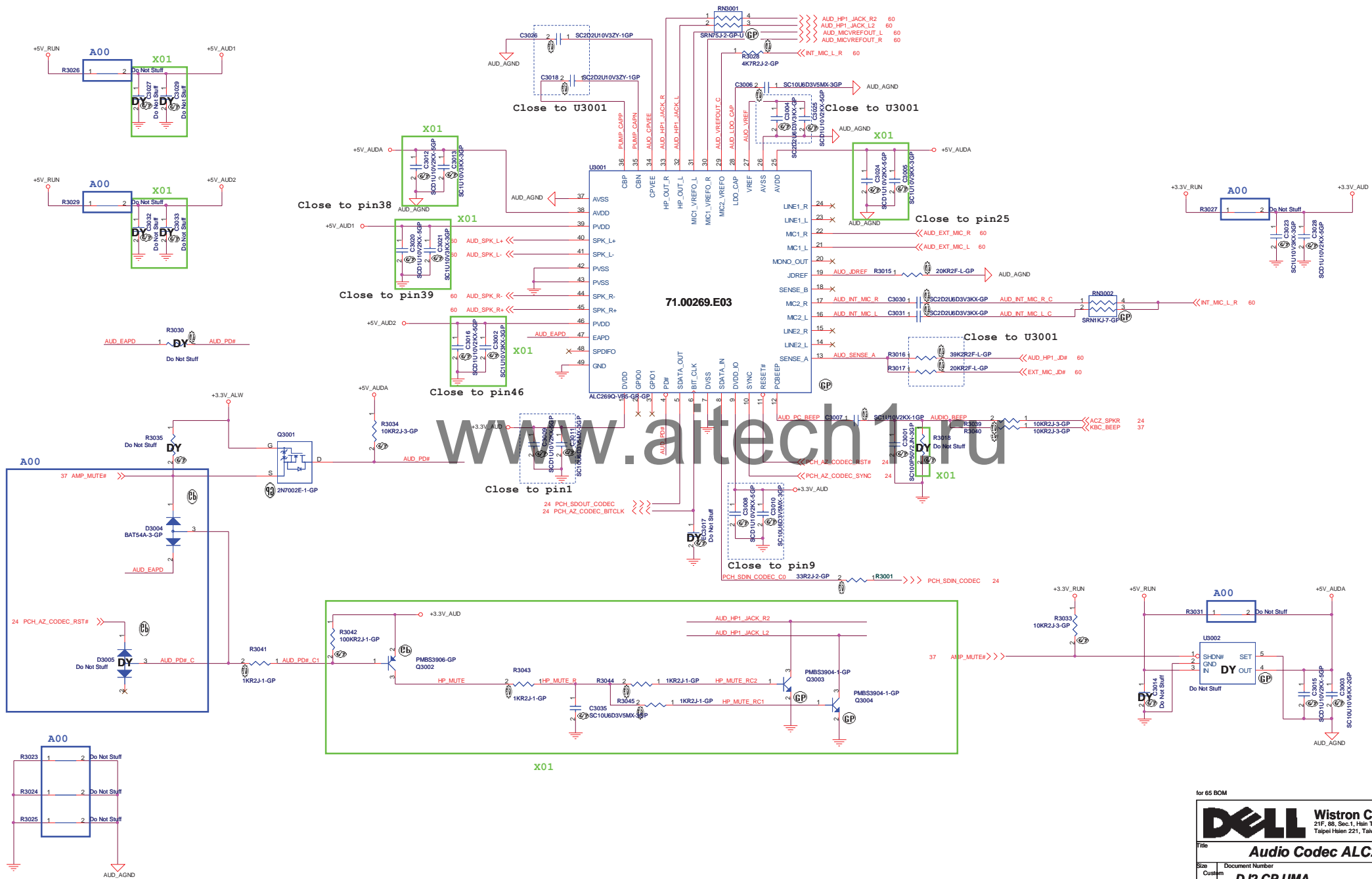
Date: Tuesday, May 18, 2010

Rev
A00

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Reserved

SSID = AUDIO



for 65 BOM



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Taipei Hsien 221, Taiwan, R.O.C.


Title	Audio Codec ALC269Q
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Size	Document Number	Rev
Custom	DJ2 CP UMA	A00
Date: Wednesday, June 02, 2010	Sheet 30 of 95	

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
DJ2 CP UMA

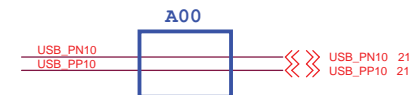
Date: Tuesday, May 18, 2010

Rev
A00

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Reserved


SSID = SDIO



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for 65 BOM



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Title

Size
A3

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Date: Tuesday, May 18, 2010

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A00


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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

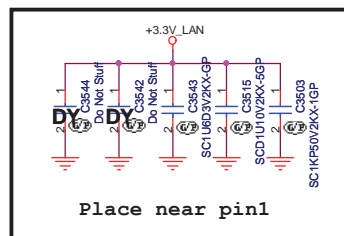
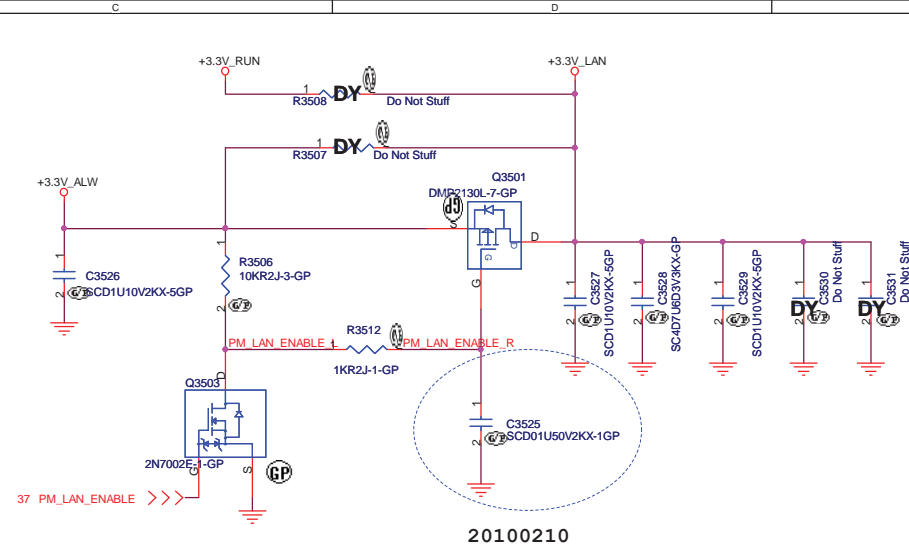
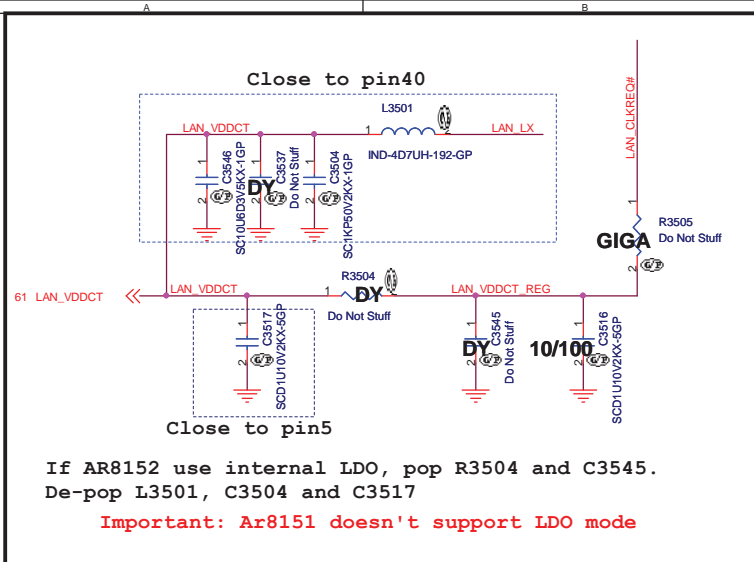
Size
A3

Document Number
DJ2 CP UMA

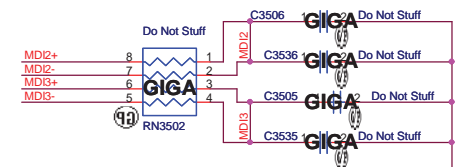
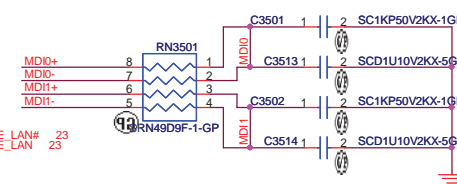
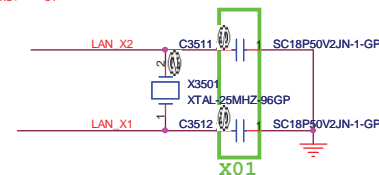
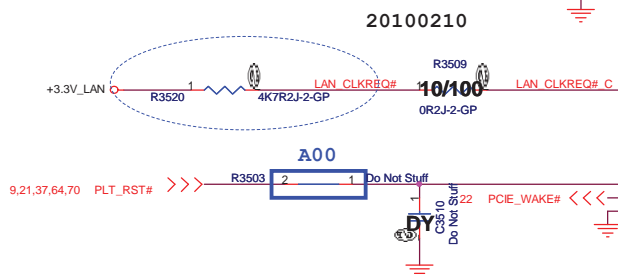
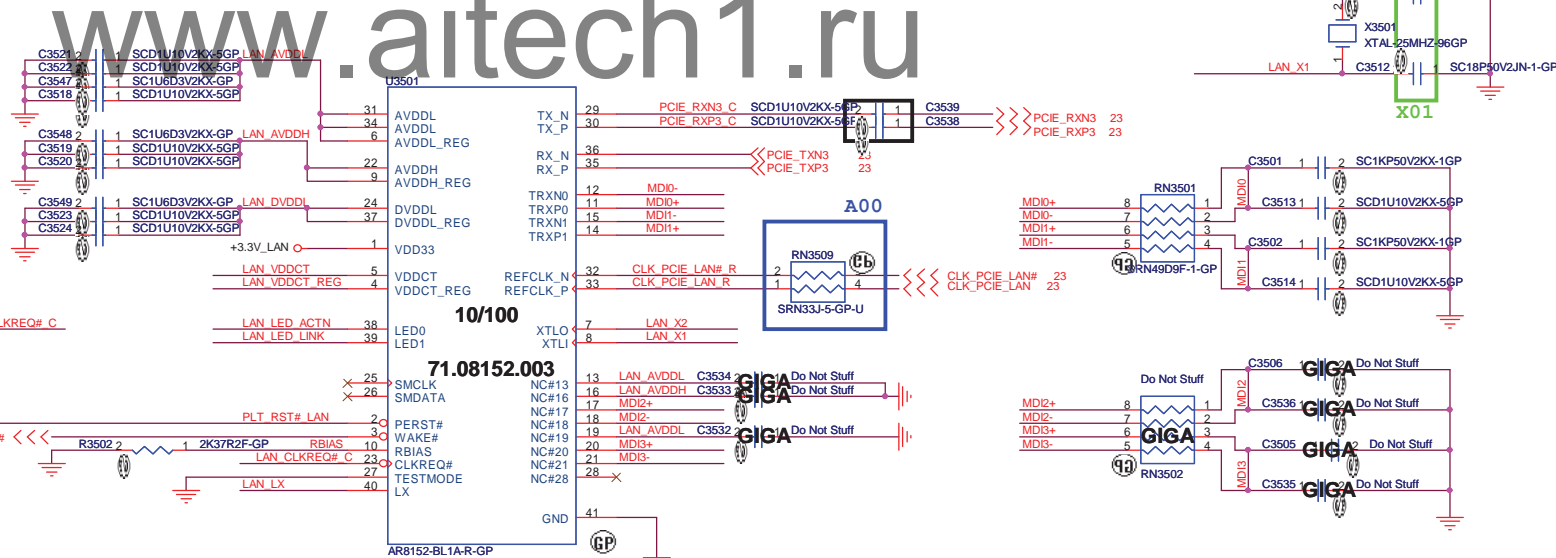
Date: Tuesday, May 18, 2010

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Rev
A00



Pin6 is the AVDDL LDO output, 1uF+0.1uF(C3547 and C3518) close to Pin6;
C3522, C3521 close to Pin31, Pin34 respectively.
Pin9 is the AVDDH LDO output, 1uF+0.1uF(C3548 and C3519) close to Pin9;
C3520 close to Pin22.
Pin37 is the DVDDL LDO output, 1uF+0.1uF(C3549 and C3523) close to Pin37;
C3524 close to Pin24.



for 65 BOM


DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title **AR8152/AR8151**
Size A3 Document Number **DJ2 CP UMA** Rev **A00**
Date: Tuesday, May 18, 2010 Sheet 35 of 95

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

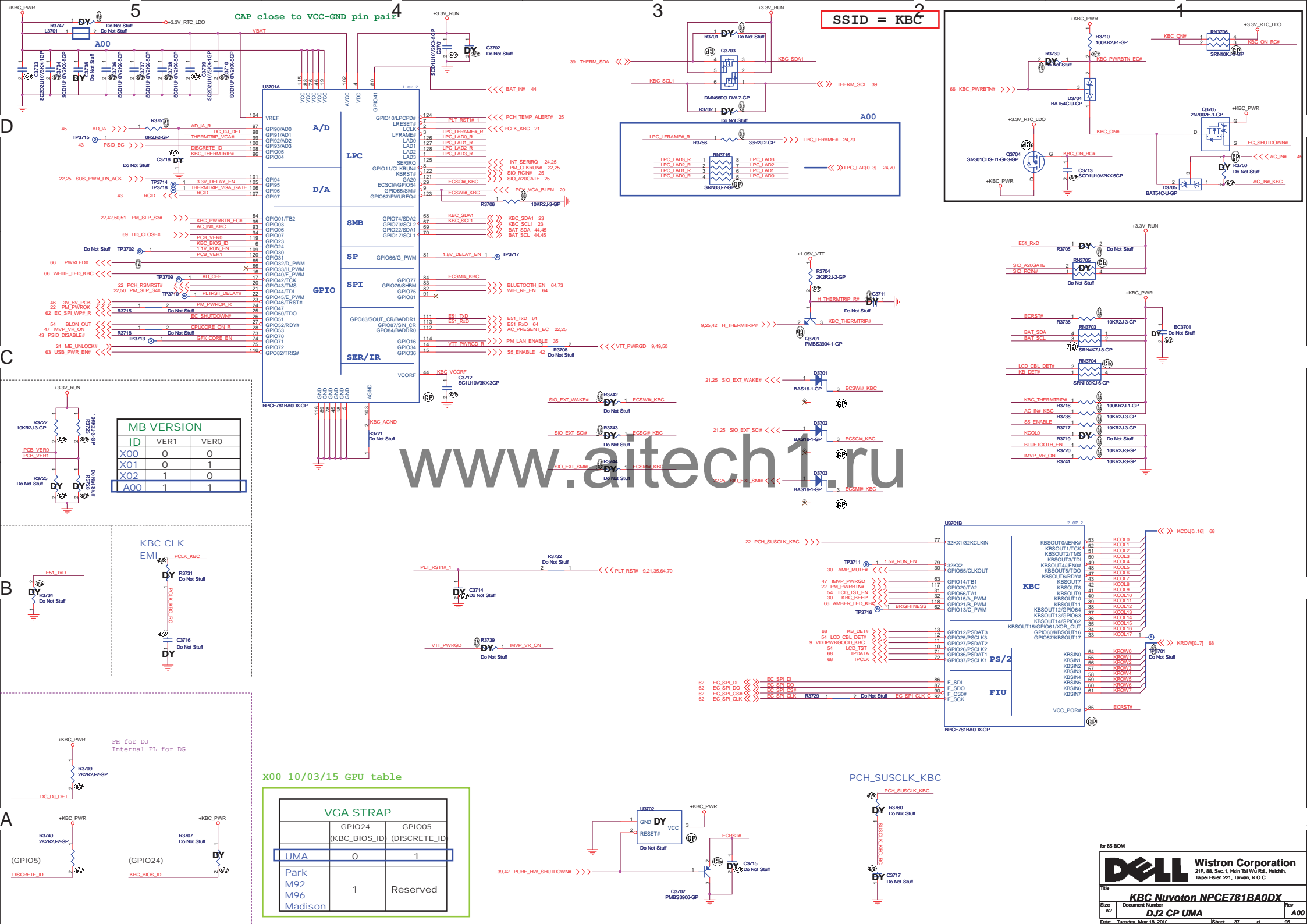
Document Number
DJ2 CP UMA

Date: Tuesday, May 18, 2010

Sheet
36

of
95


Rev
A00



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for 65 BOM



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Title

Reserved

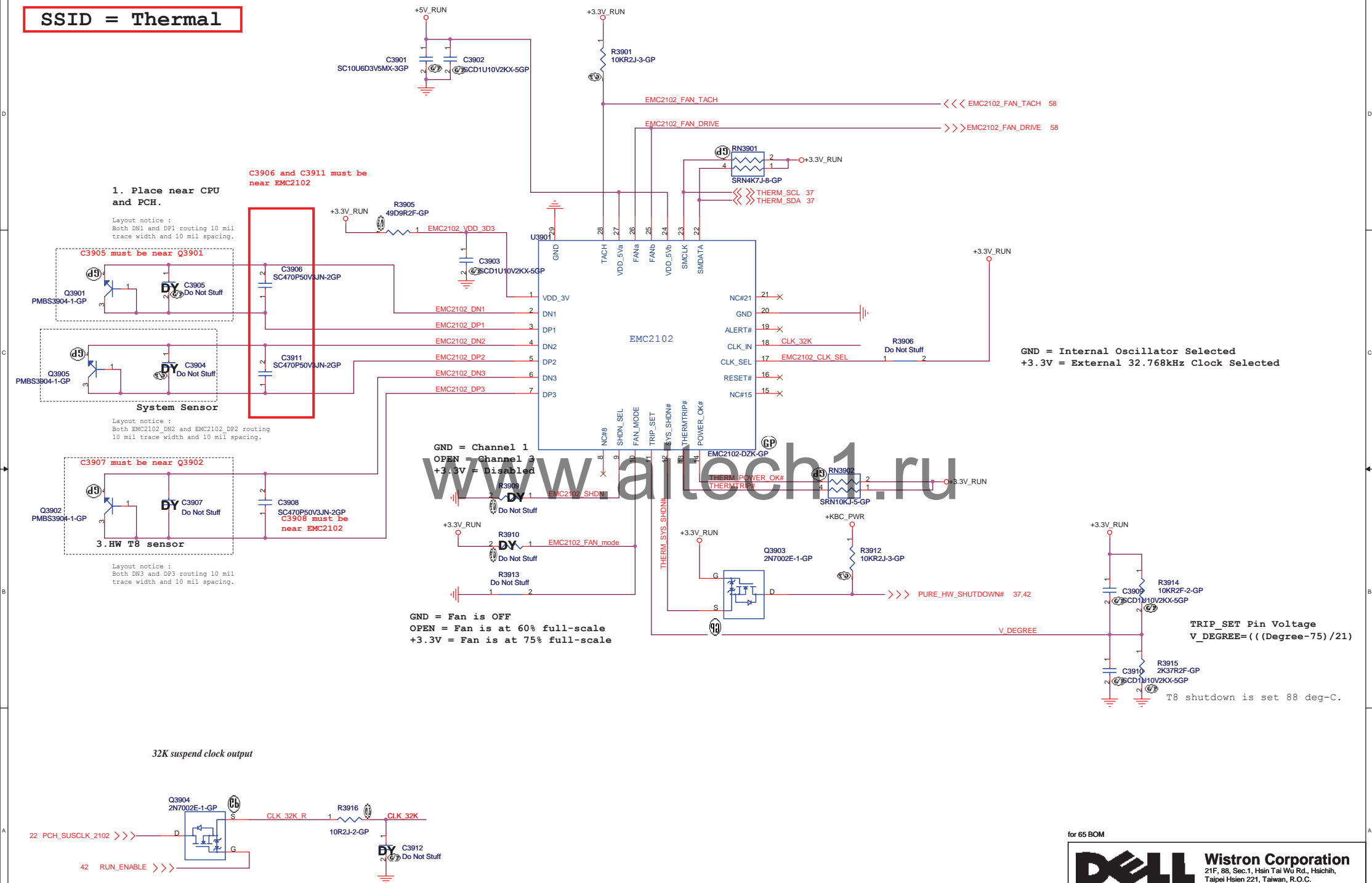
Size
A3

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DJ2 CP UMA

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SSID = Thermal



for 65 BOM



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Title

Thermal/Fan Controller EMC2102

Size	Document Number
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Custom **DJ2 CP UMA**

Date: Tuesday, May 18, 2010


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for 65 BOM



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Title

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A3

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DJ2 CP UMA

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Title

Reserved

Size
A3

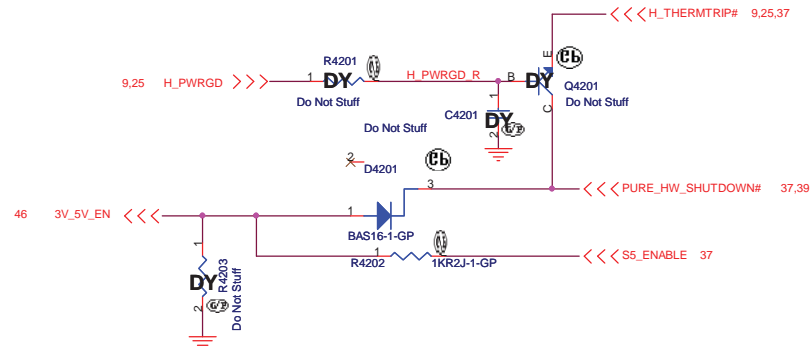
Document Number
DJ2 CP UMA

Date: Tuesday, May 18, 2010

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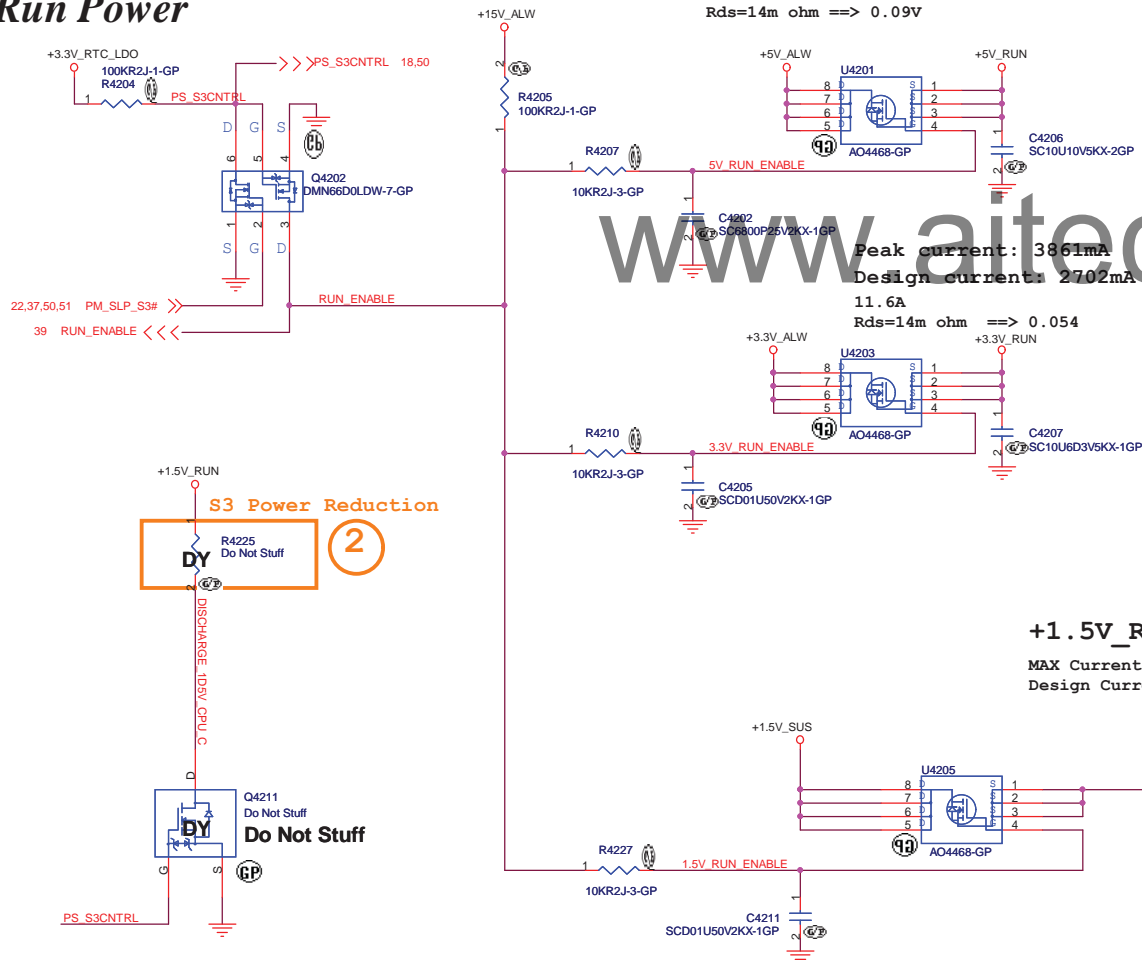
Rev
A00

SSID = Reset.Suspend



Peak current: 6370mA (HD:1100 ODD:2500)
Design current: 4459 mA
11.6A
Rds=14m ohm ==> 0.09V

Run Power



Peak current: 3861mA
Design current: 2702mA
11.6A
Rds=14m ohm ==> 0.054

+1.5V_RUN


MAX Current 3000 mA
Design Current 2100 mA

+1.5V_RUN_CPU Consumption
Peak current 3A

+1.5V_RUN for Mini-Card Consumption
Peak current 1A

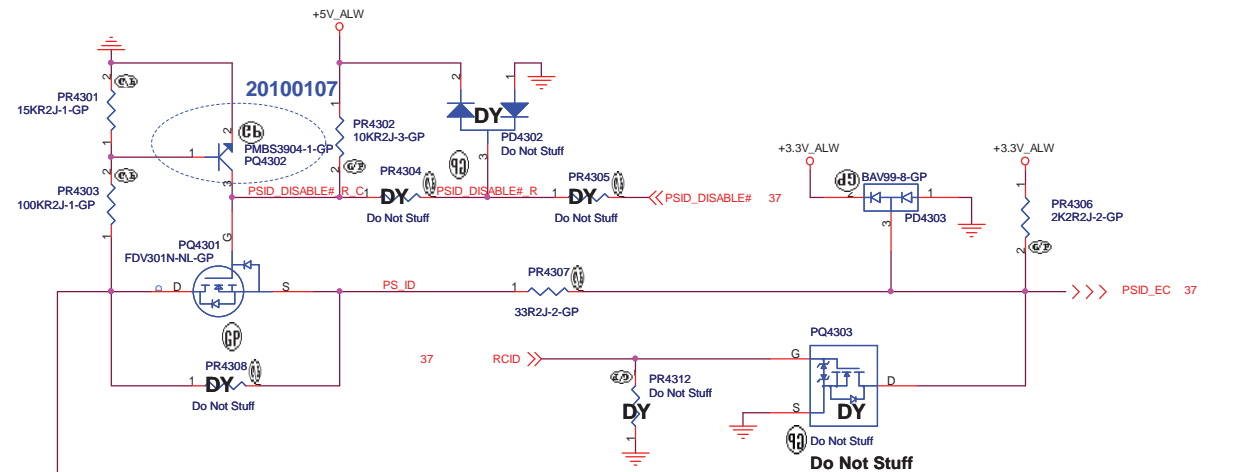
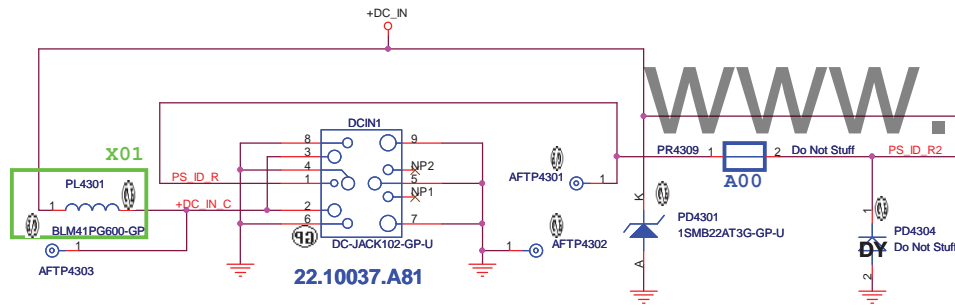
Total= 4A

for 65 BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Power Plane Enable</i>			
Size A3	Document Number	Rev	
	<i>DJ2 CP UMA</i>	<i>A00</i>	
Date:	Tuesday, May 18, 2010	Sheet 42 of 95	

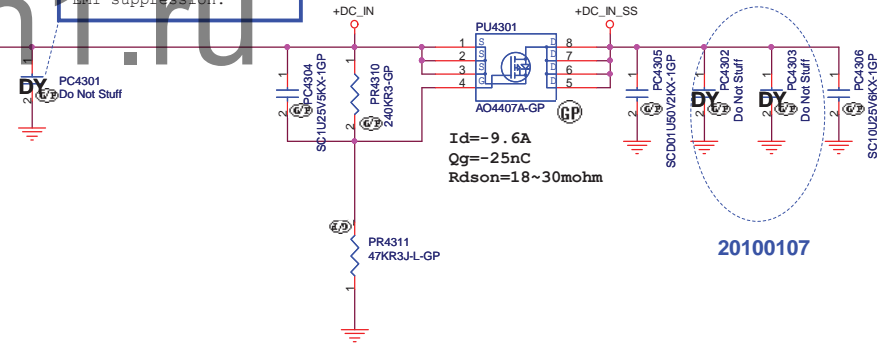
SSID = PWR.Support

DCin CONN



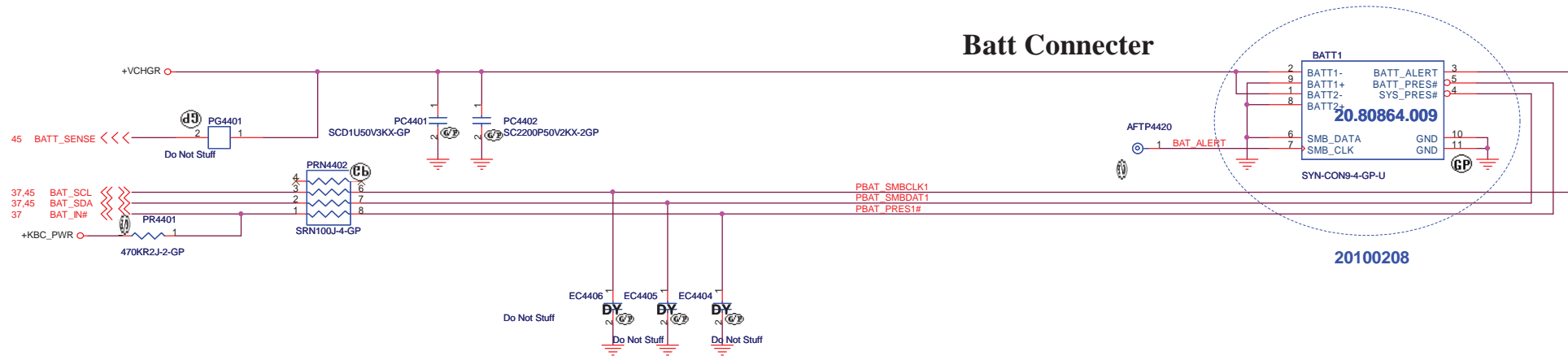
When PQ4301 is stuffed, the PR4306 need change to 2.2K 1% resistor

This cap should be used only as last resort for EMI suppression.

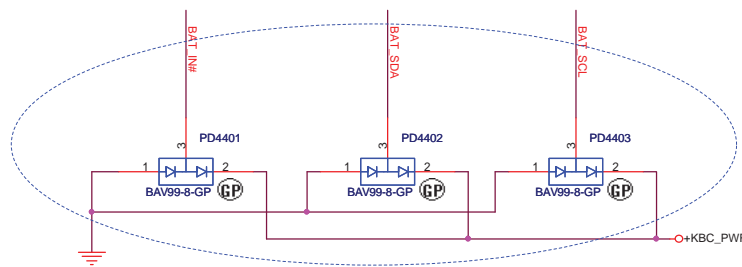
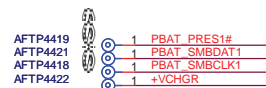


for 65 BOM

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EC404,EC405,EC406 Close BATT1 Connector

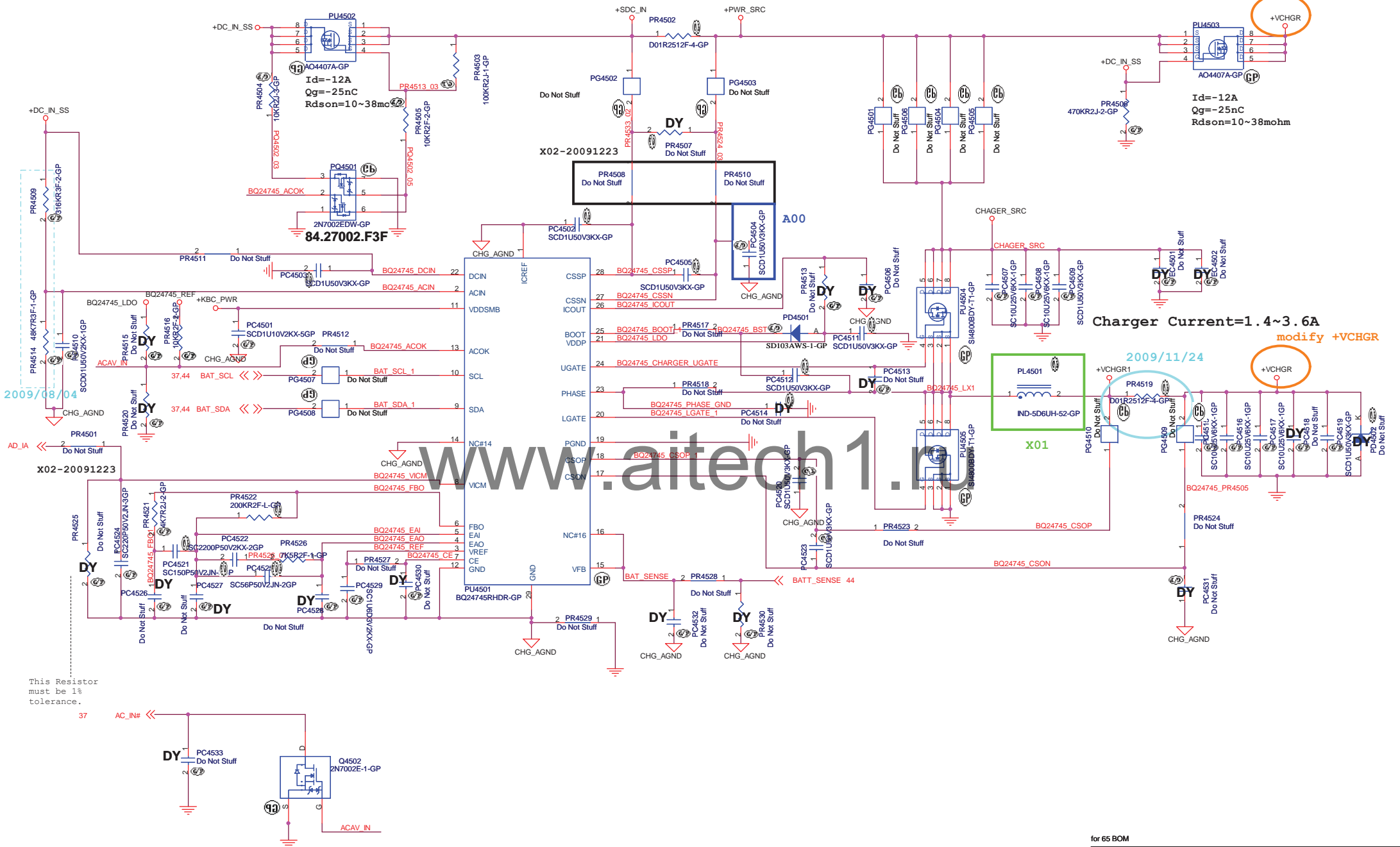


for 65 BOM

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			BATT CONN	
Size	Document Number	Rev		
A3	DJ2 CP UMA	A00		
Date:	Tuesday, May 18, 2010	Sheet	44	of 95

SSID = Charger



for 65 BOM

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CHARGER BQ24745			
Size	Document Number	Rev	
Custom	DJ2 CP UMA	A00	
Date:	Tuesday, May 18, 2010	Sheet	45 of 95

Design Current = 8.12A
10.56A < OCP < 13.6A

Design Current = 7.3A
9.49A < OCP < 12.41A

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TPS51125	CH1	CH2
T0NSEL	200kHz	265kHz
GND	245kHz	305kHz
VREF3	300kHz	375kHz
VREF5	365kHz	460kHz

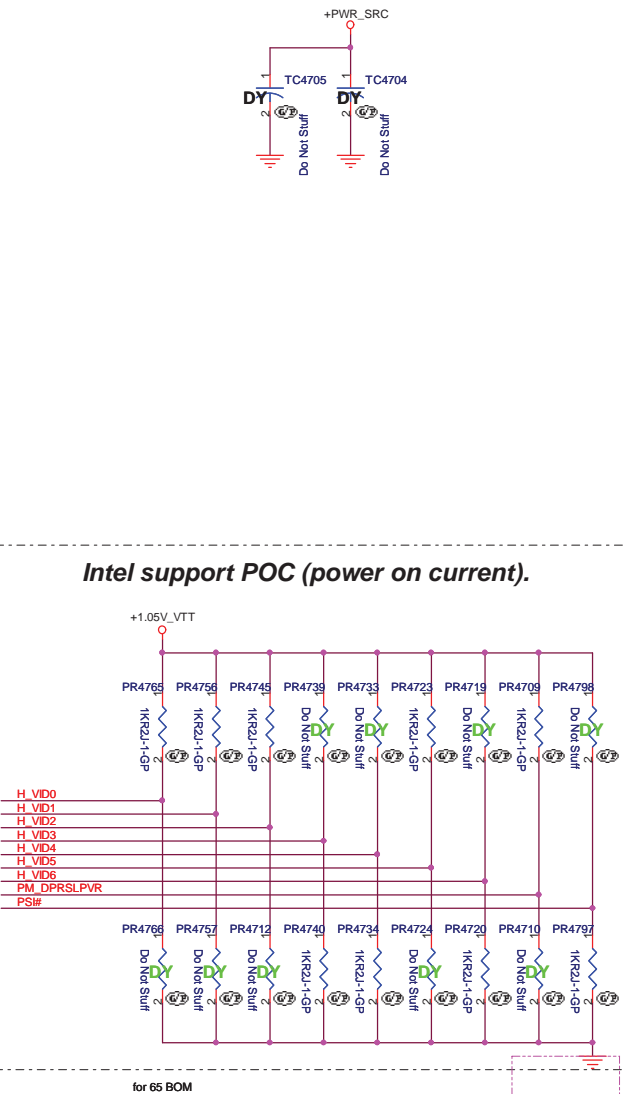
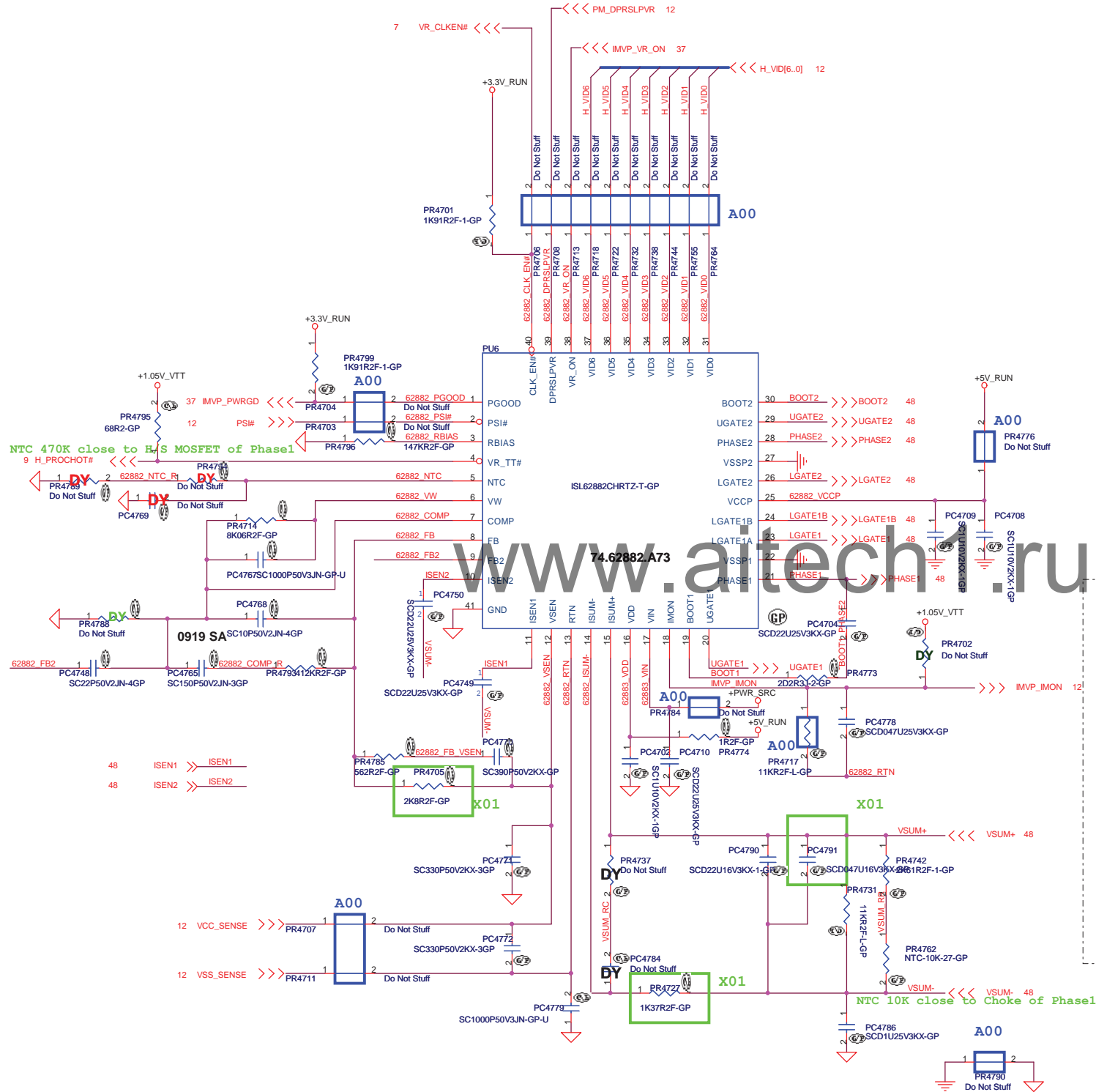
TPS2205B	CH1	CH2
T0NSEL	200kHz	250kHz
GND	300kHz	375kHz
VREF3	365kHz	460kHz
VREF5	365kHz	460kHz

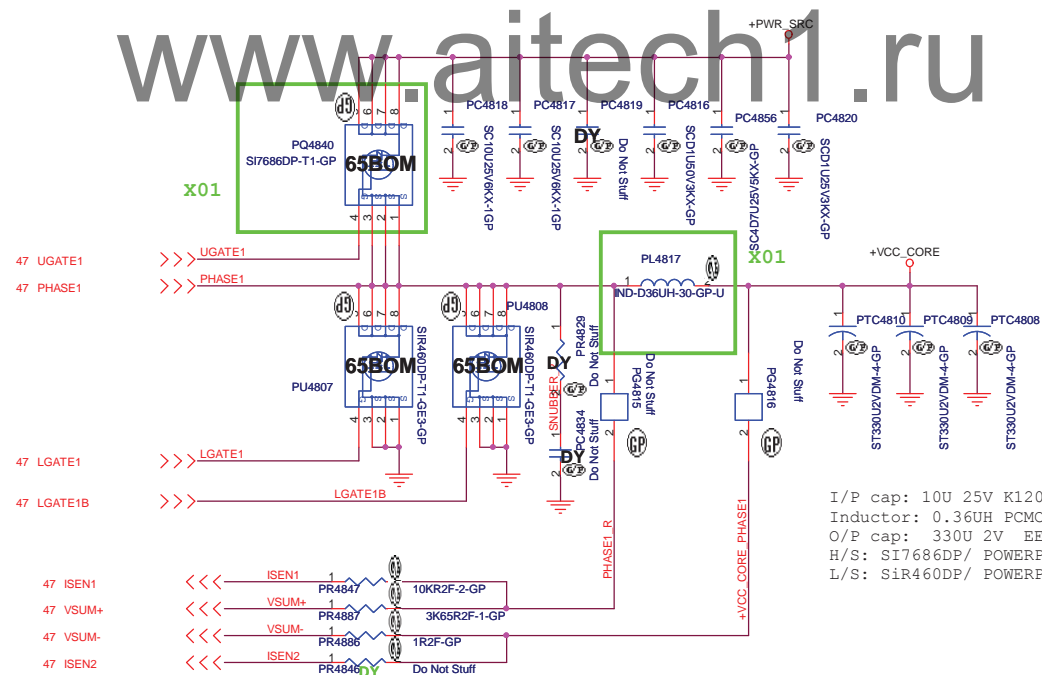
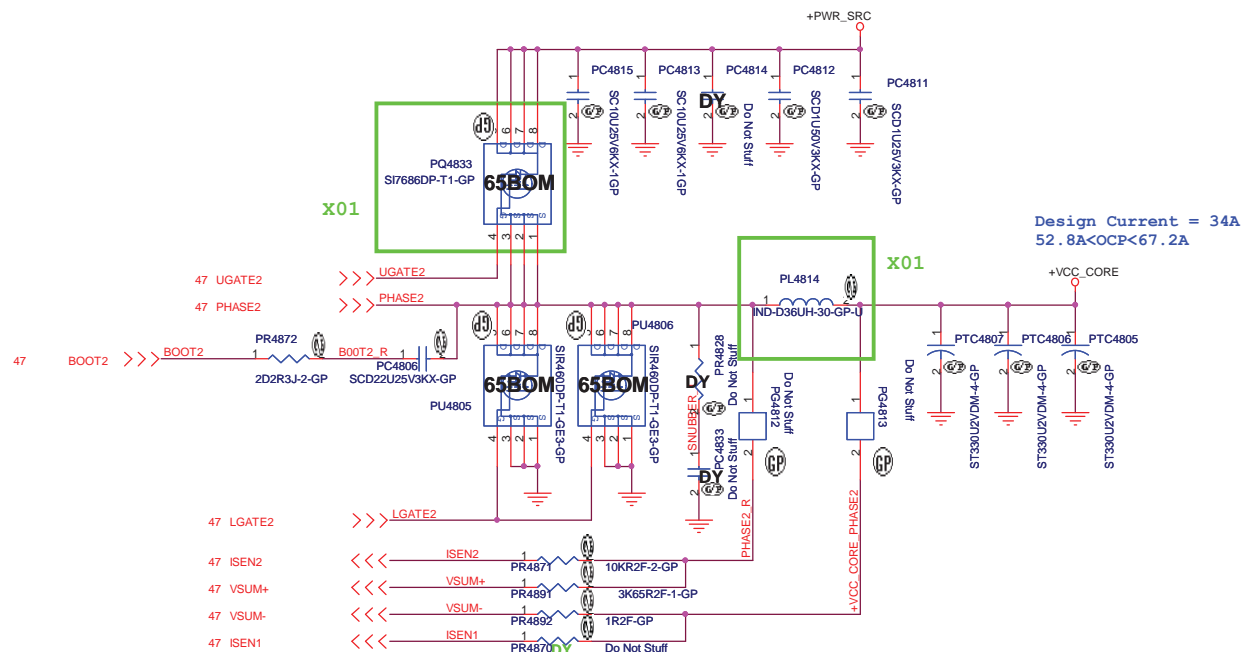
I/P cap: 100 25V K1206 X5R/ 78.10622.52L
Inductor: 3.30H PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEP5LB20J107M(45) 8R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 SO-8/ 23mohm/30mohm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mohm@4.5Vgs/ 84.06690.E37

by 65 BOM

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
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Title: **TPS51125 5V/3D3V**
Size: A2 Document Number: **DJ2 CP UMA** Rev: A00
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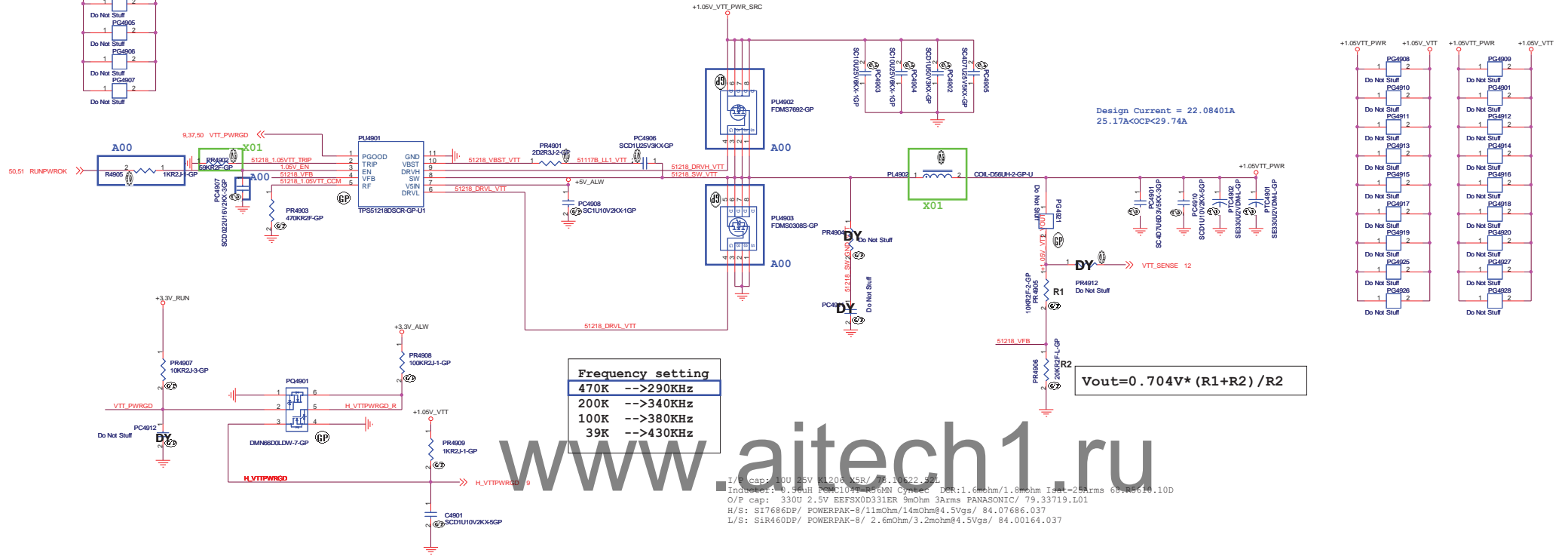




for 65 BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title ISL62883 CPU CORE	
Size A3	Document Number DJ2 CP UMA	Rev A00	
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TPS51218 for +1.05V_VTT



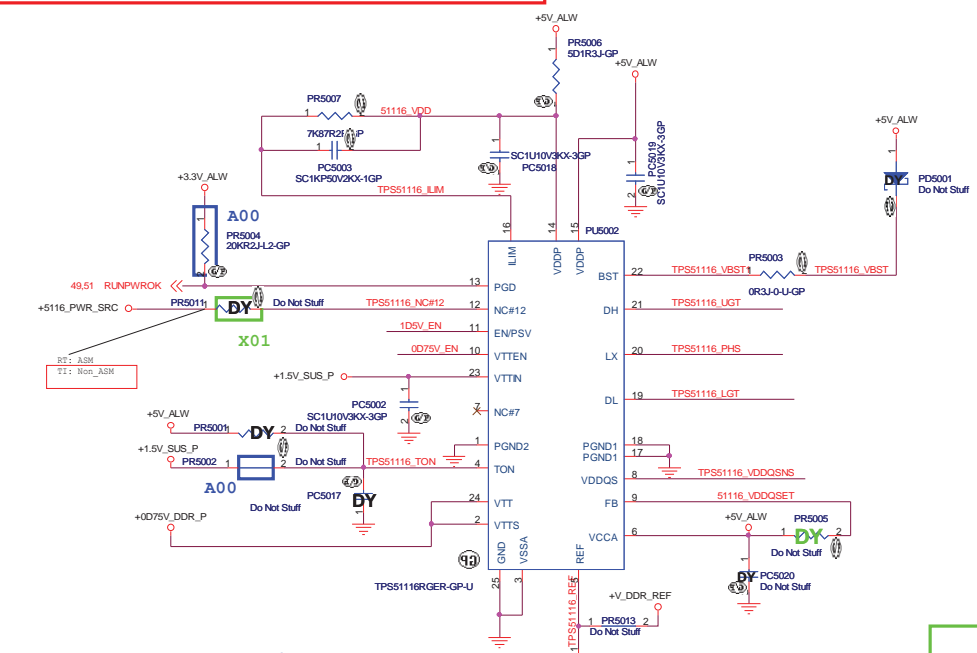
Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/F cap: 100 25V K1204 X5/ 10.1022 30L
 Inductor: 0.5uH POWD104-R56MN C/ntec DRR:1.6mhm/1.8mhm Isat=25Arms 68.86610.10D
 O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
 H/S: S17686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
 L/S: S1R460DP/ POWERPAK-8/ 2.6mOhm/3.2mOhm@4.5Vgs/ 84.00164.037

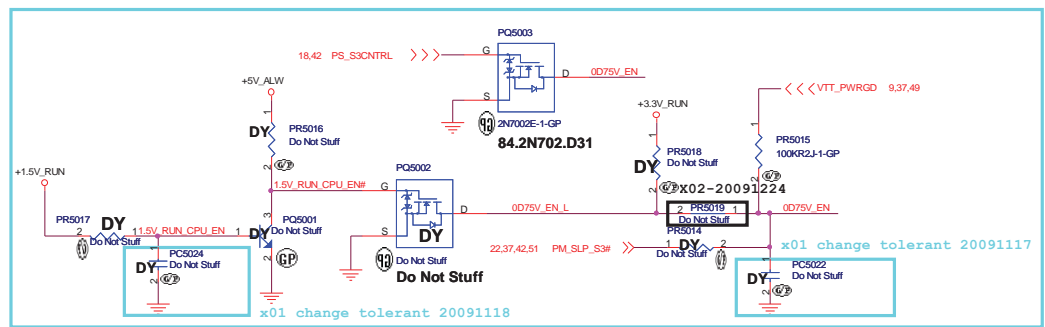
for B5 BOM

SSID = PWR.Plane.Regulator_1p5v0p75v

5 S3 Power Reduction X01 20091111



Design Current = 0.7A

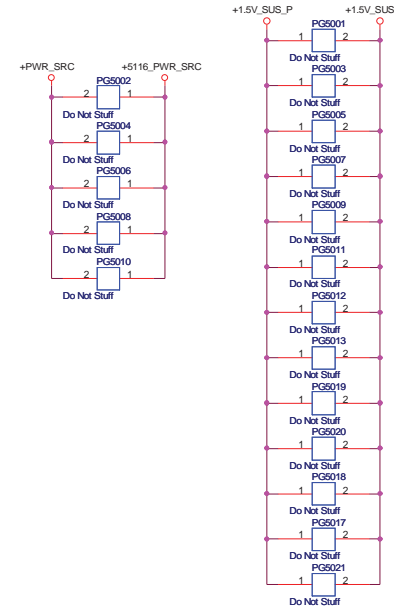


Design Current = 10.51A
13.66A<OCP< 17.88A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5uH PCMC104T-1R5 Cyntec DCR:3.8mohm Isat=33Arms 68.1R510.10J
O/P cap: 220U 2V BEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/ 11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq->>400KHz



for 65 BOM

**Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title
TPS51116 +1.5V SUS

Size
Custom

Document Number
DJ2 CP UMA

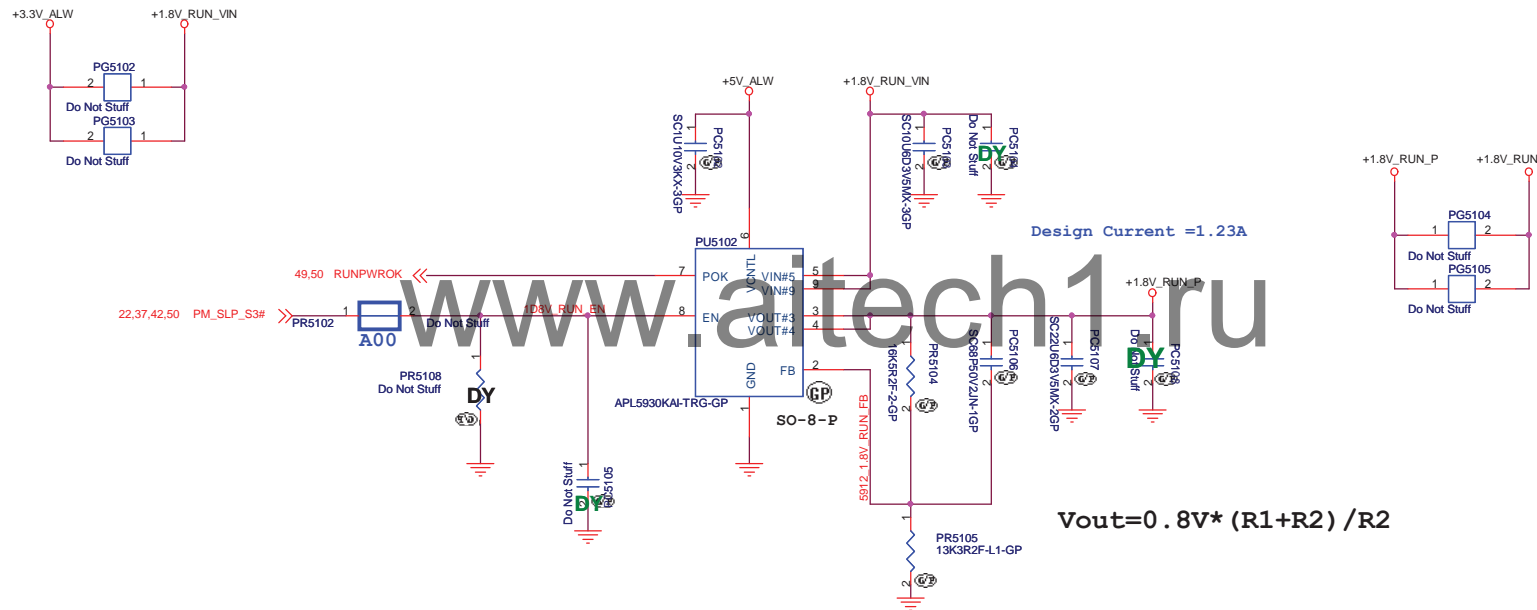
Date: Tuesday, May 18, 2010

Rev
A00

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SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN




for 65 BOM

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
APL5930 +1.8V RUN			
Size	Document Number	Rev	
A3	DJ2 CP UMA		A00
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for 65 BOM



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

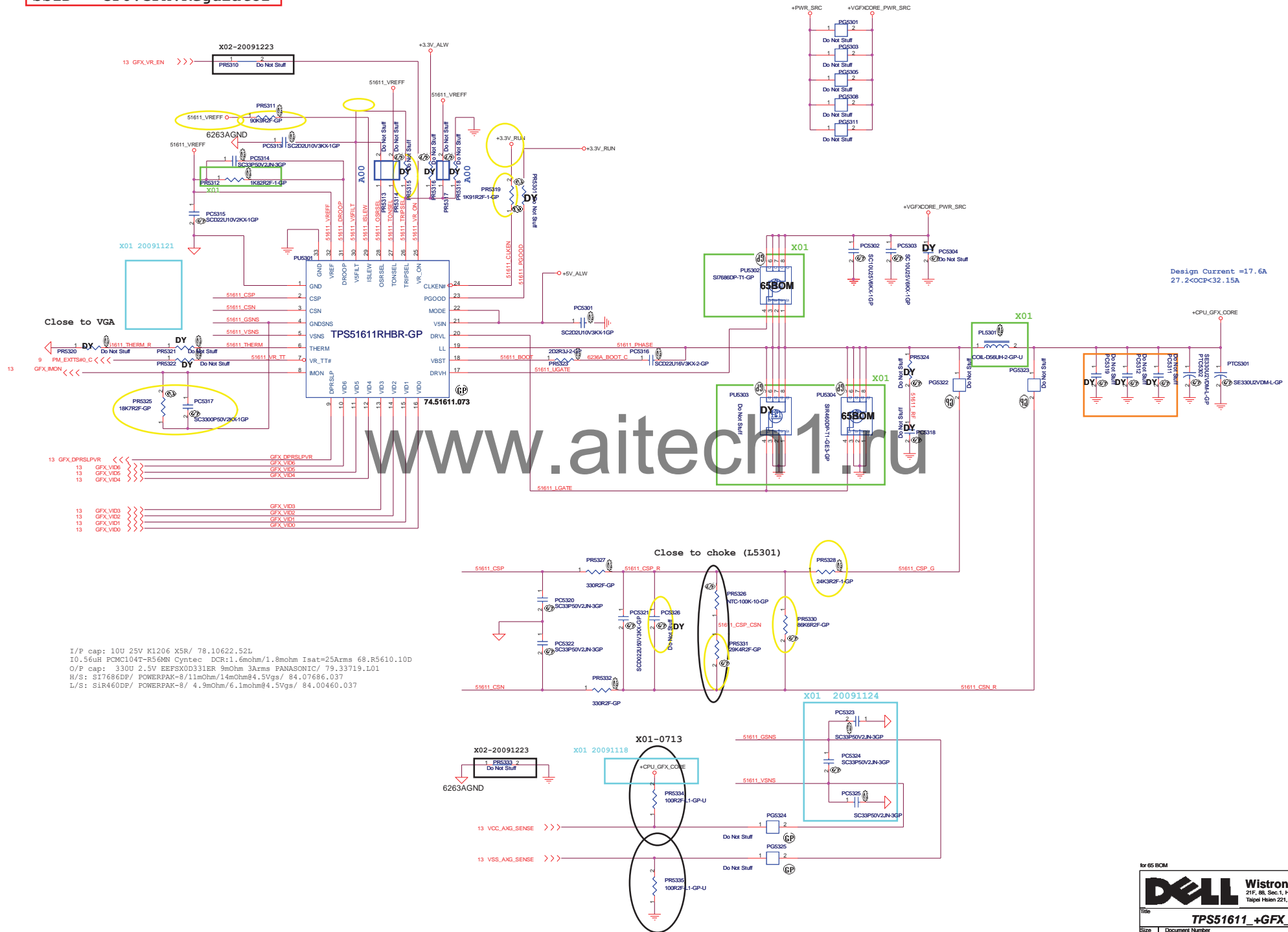
Document Number
DJ2 CP UMA

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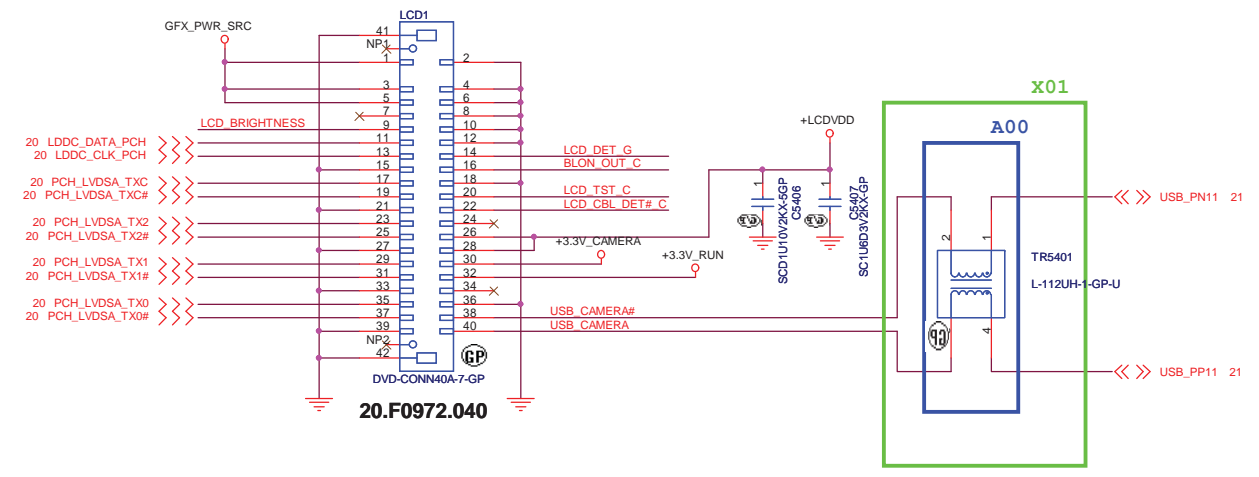
SSID = CPU.GFX.Regulator



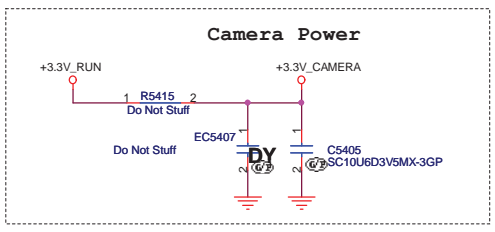
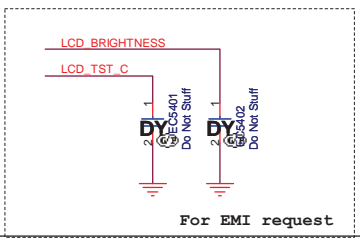
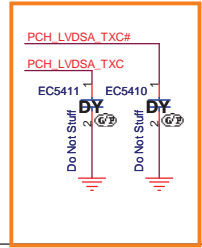
for 65 BOM

SSID = VIDEO

LVDS CONNECTOR

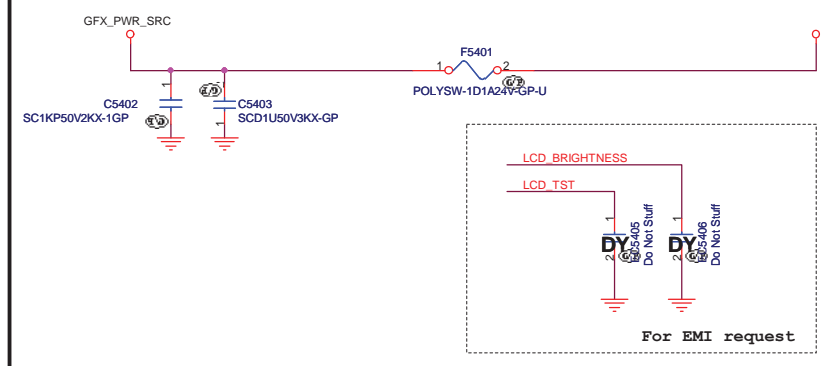


Close to LVDS connector



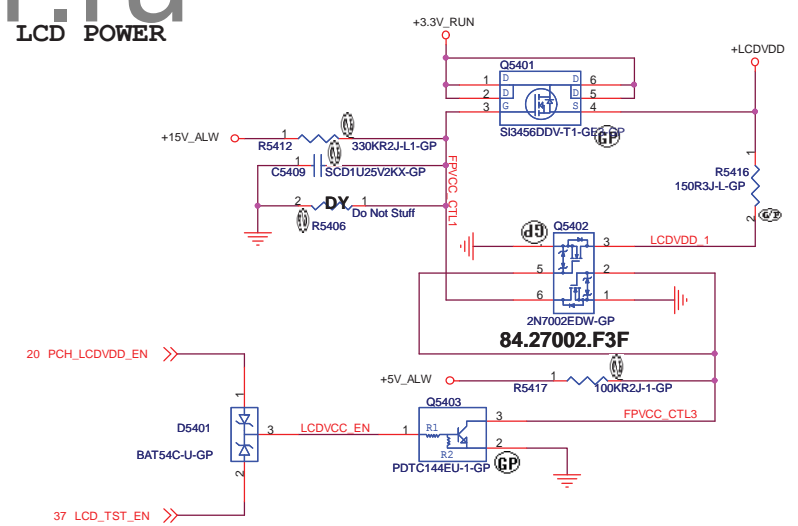
SSID = Inverter

INVERTER POWER



SSID = VIDEO

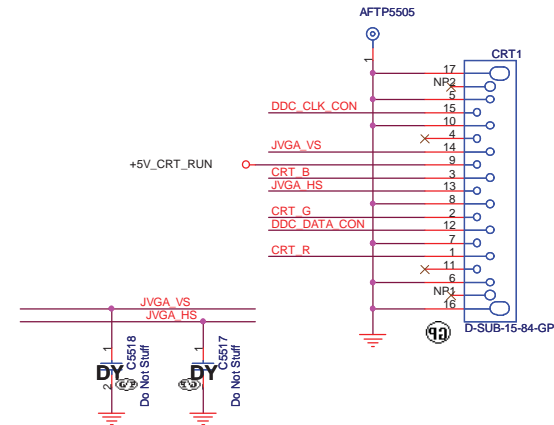
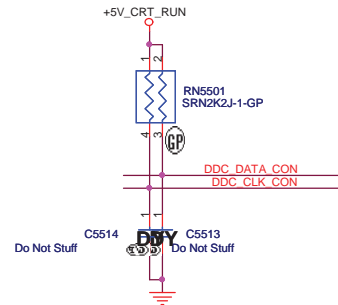
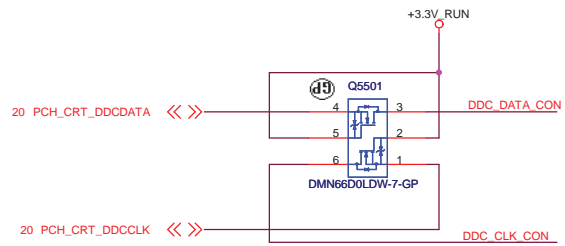
LCD POWER



for 65 BOM

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LCD/Inverter Connector				
Size A3	Document Number DJ2 CP UMA			Rev A00
Date: Tuesday, May 18, 2010		Sheet 54 of 95		

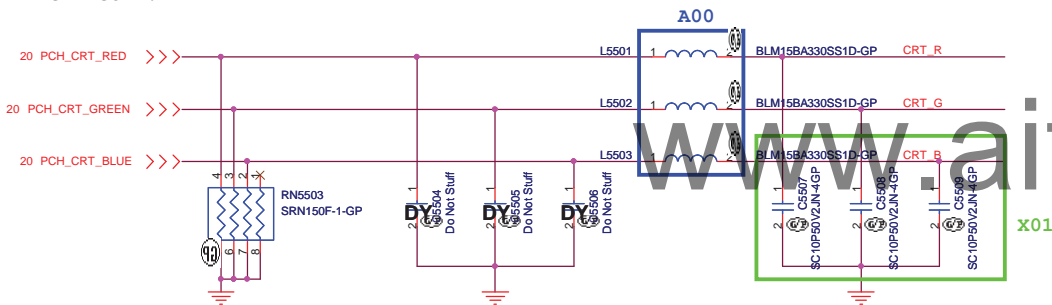
SSID = VIDEO



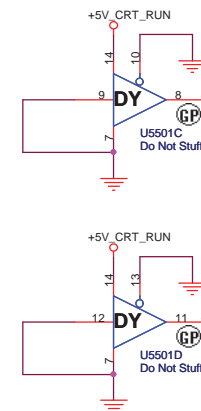
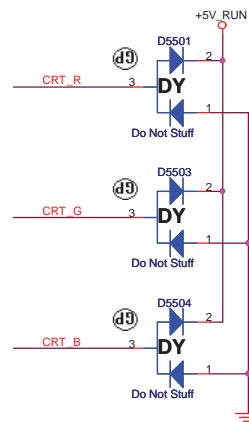
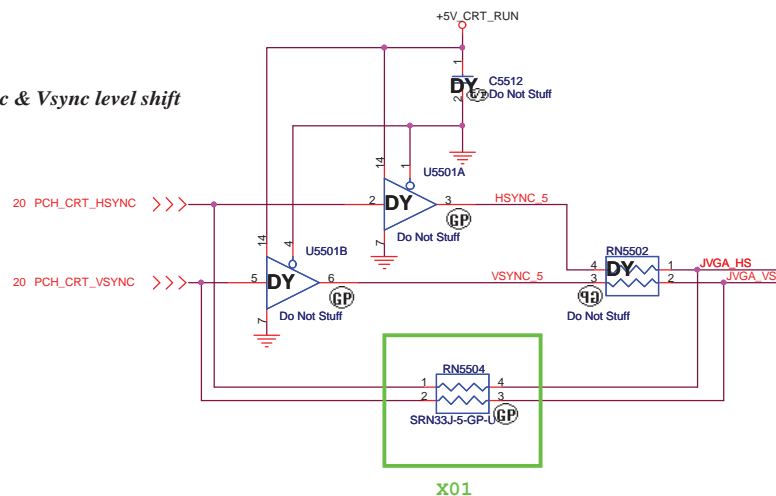
Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

AFTP5501	1	+5V_CRT_RUN
AFTP5506	1	DDC_DATA_CON
AFTP5503	1	DDC_CLK_CON
AFTP5506	1	CRT_R
AFTP5507	1	CRT_G
AFTP5504	1	CRT_B
TP5505	1	JVGA_HS
TP5505	1	JVGA_VS



Hsync & Vsync level shift




for 65 BOM

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT Connector			
Size	Document Number	Rev	A00
Date:	Tuesday, May 18, 2010	Sheet 55 of 95	

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for 65 BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
DJ2 CP UMA

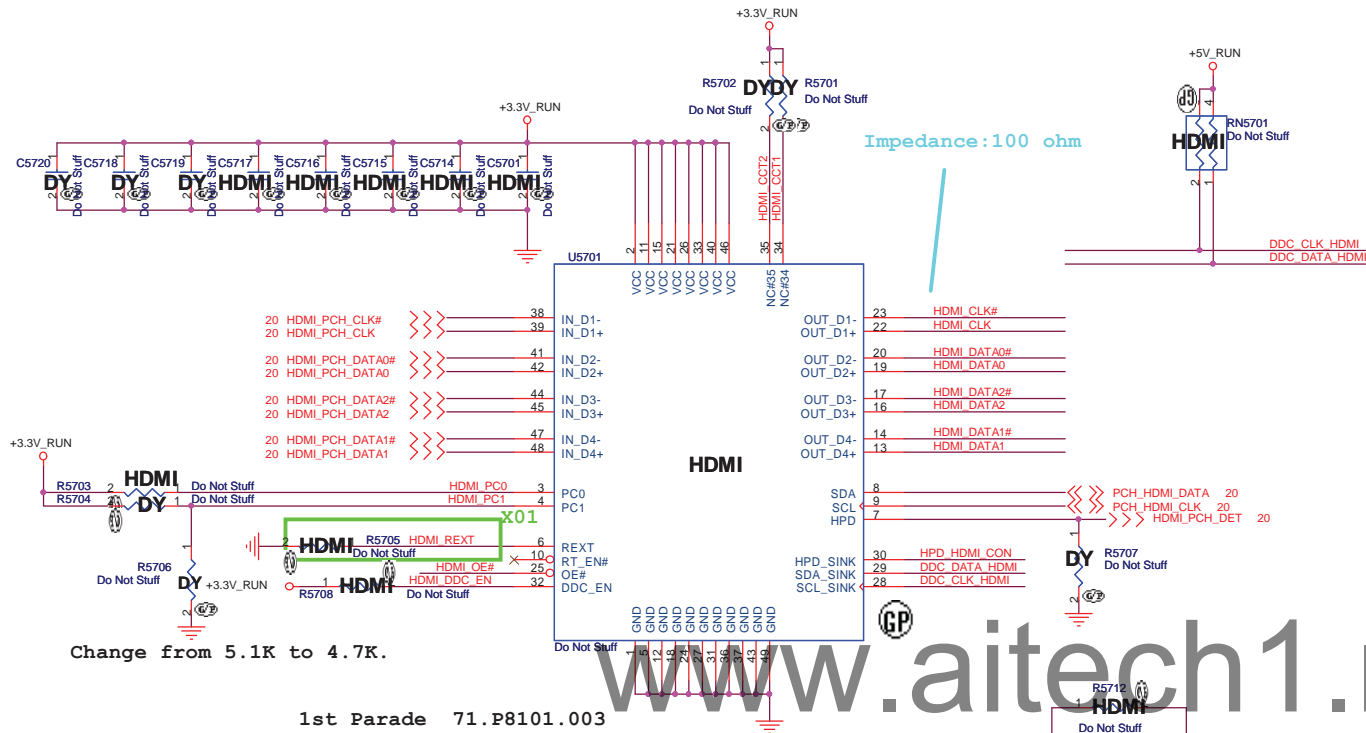
Date: Tuesday, May 18, 2010

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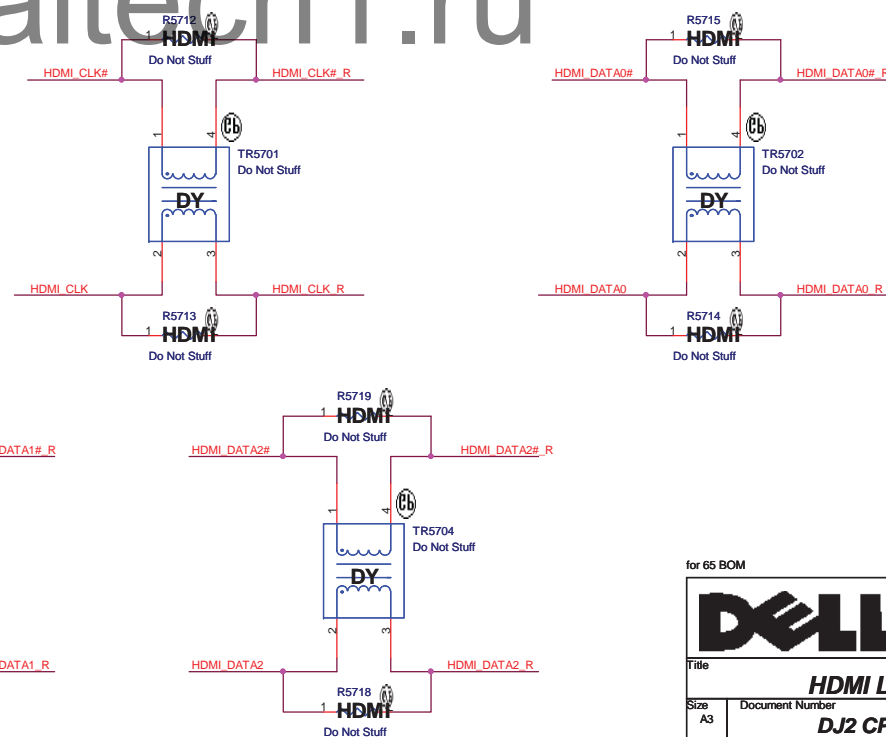
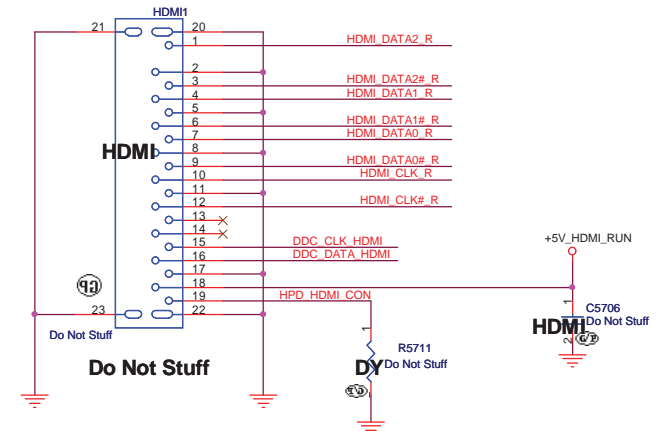
Rev
A00

SSID = VIDEO

HDMI Level Shifter & CONNECTOR



HDMI CONN



x01 change tolerant 20091117

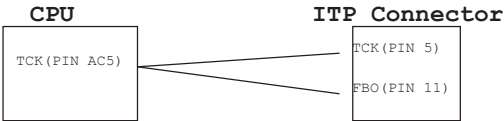
for 65 BOM

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: HDMI Level Shift/ Connector			
Size: A3	Document Number: DJ2 CP UMA	Rev: A00	
Date: Tuesday, May 18, 2010		Sheet: 57	of: 95

SSID = User.Interface

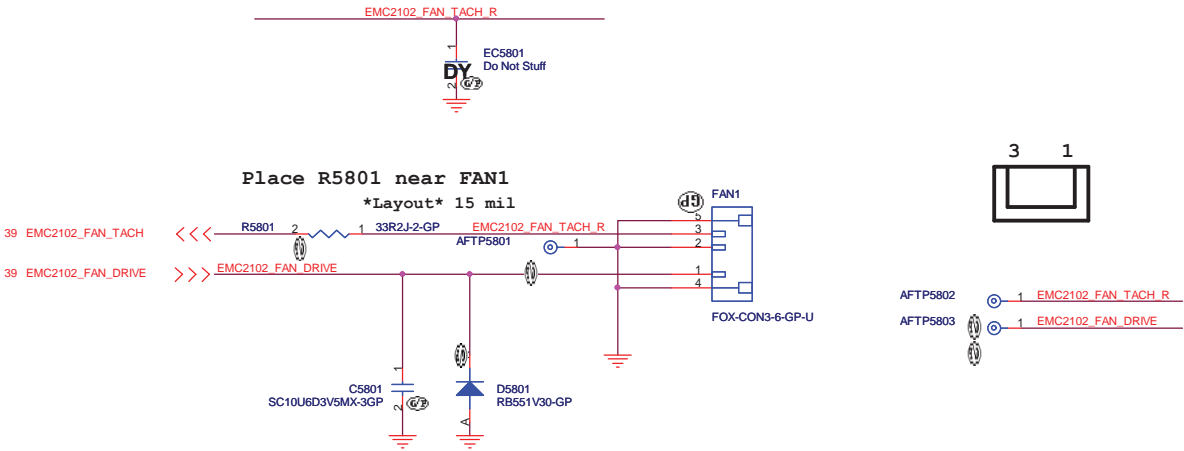
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



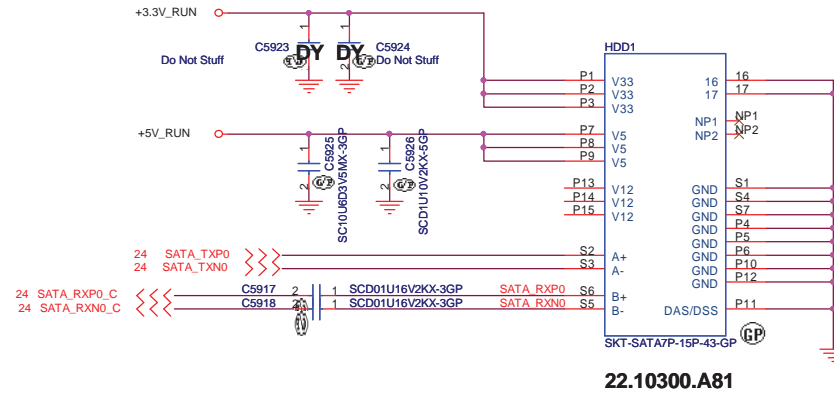
SSID = Thermal

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Fan Connector



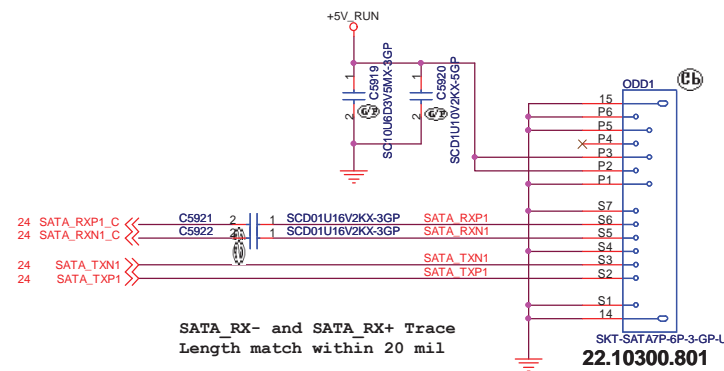
SSID = SATA

SATA HDD Connector



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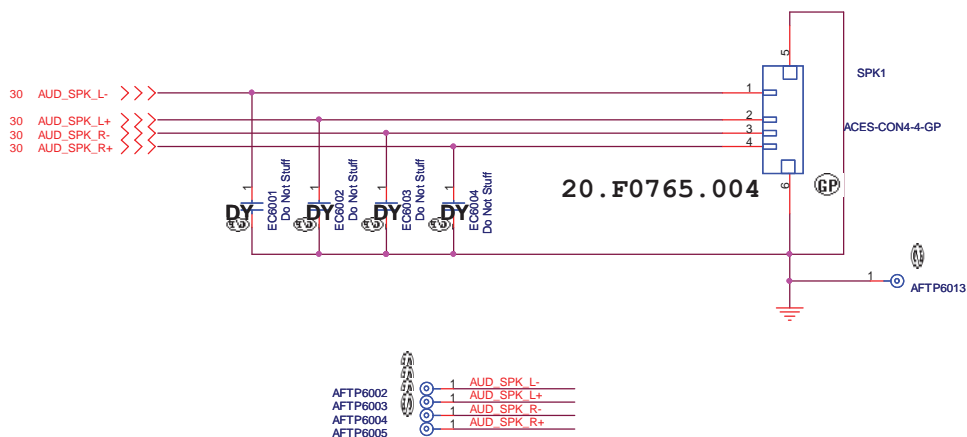
SATA ODD Connector



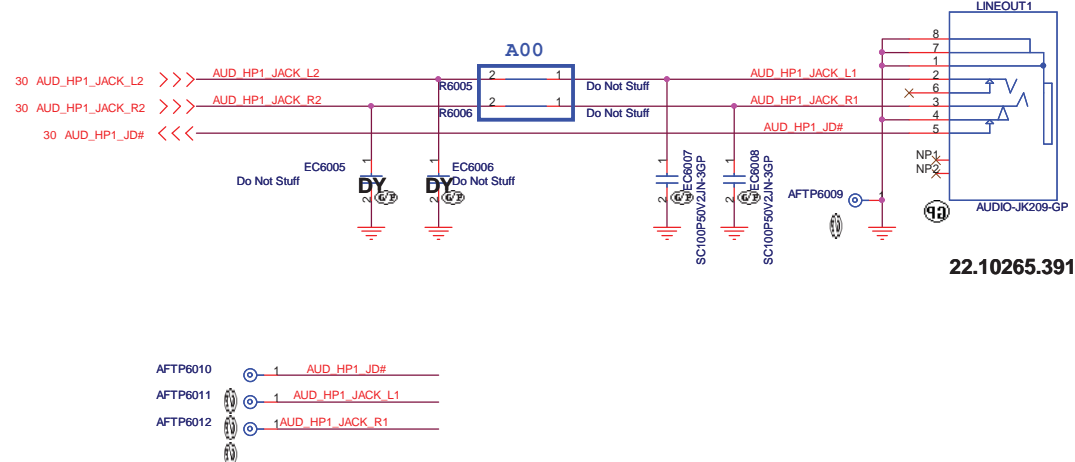
for 65 BOM

SSID = AUDIO

Speaker Connector



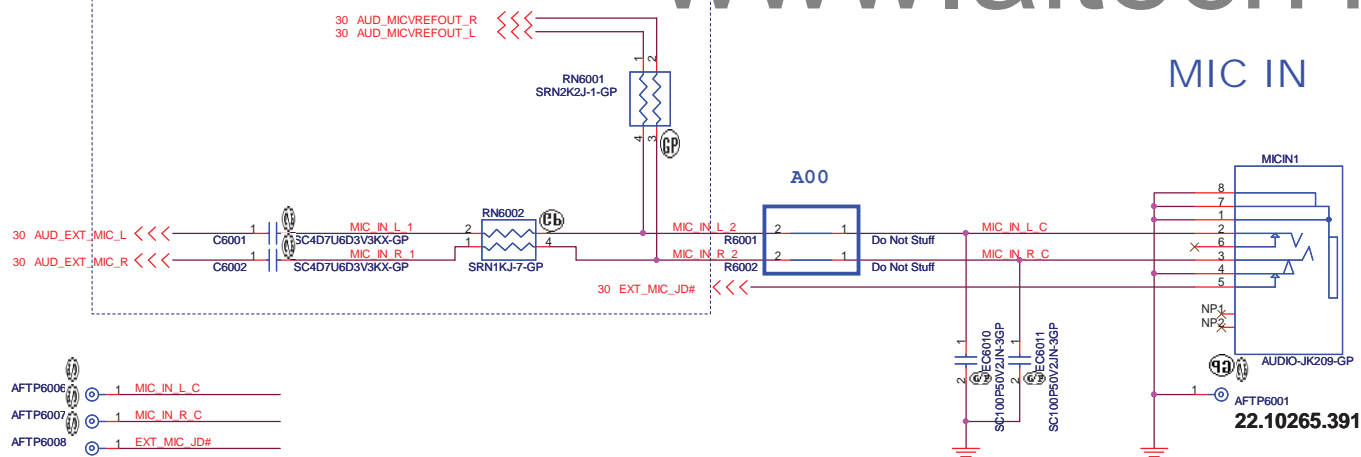
LINE1 OUT



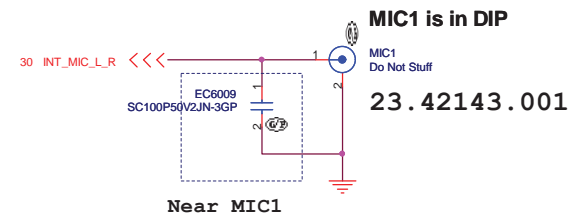
Plase thise parts near codec

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MIC IN



Internal Microphone



for 65 BOM

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Audio Jack
Size A3 Document Number
Chelsea DJ2 AMD UMA Rev
A00
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1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

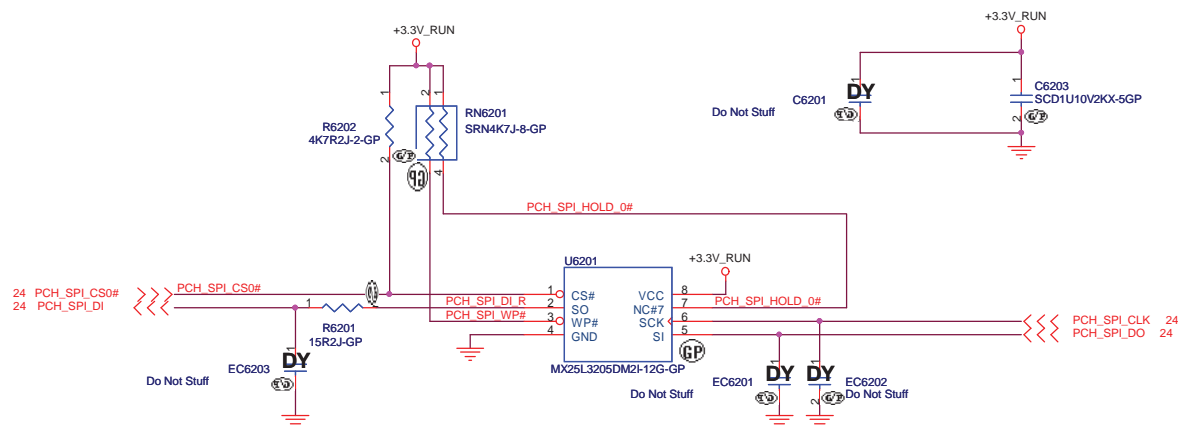
10/100M Lan Transformer



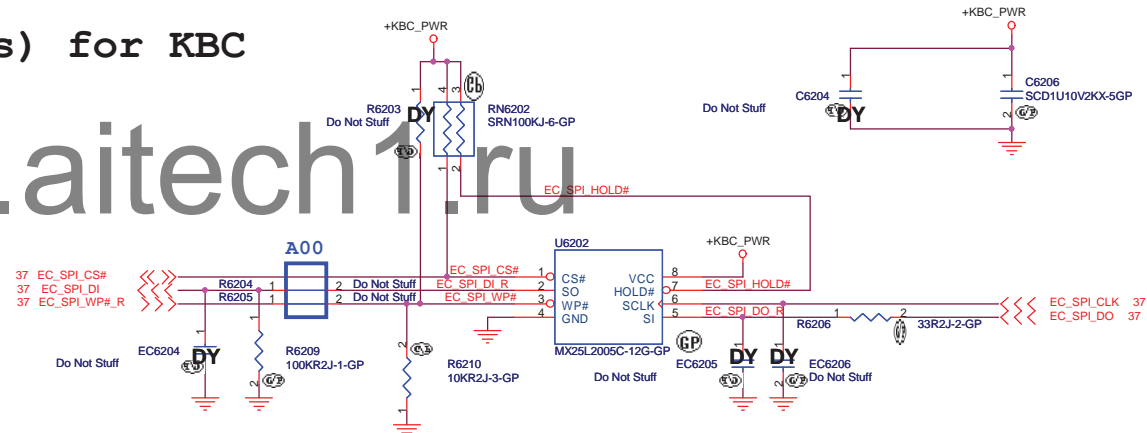
Title			
XFORM/RJ45			
Size	Document Number	Rev	
A3	DJ2 CP UMA	A00	
Date:	Tuesday, May 18, 2010	Sheet 61 of	95

SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

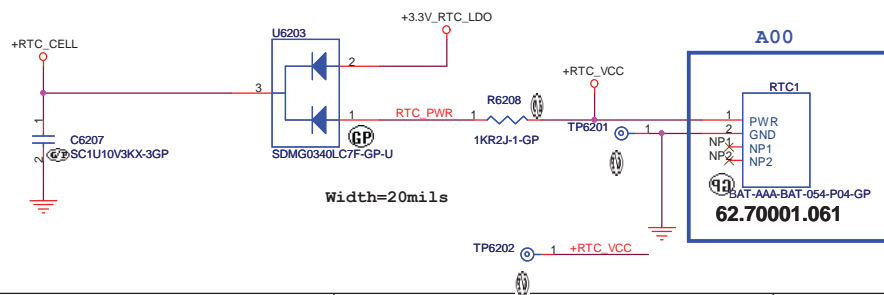


SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector



for 65 BOM



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTC

Size
A3

Document Number

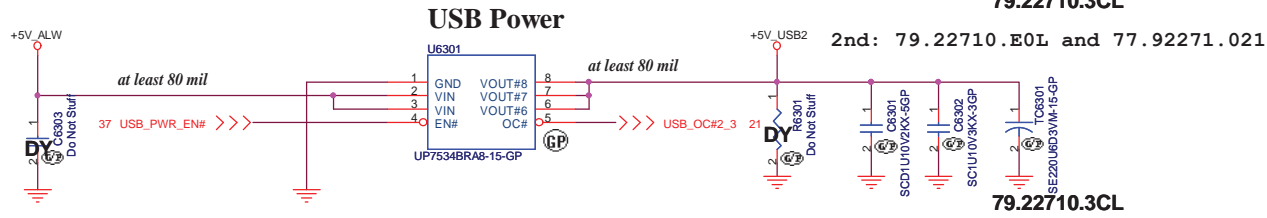
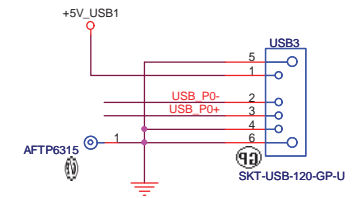
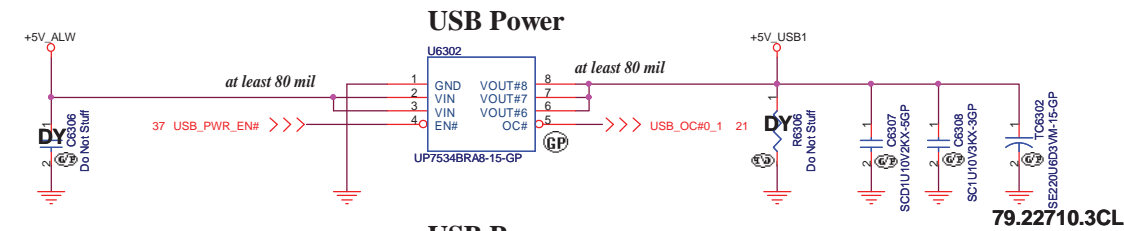
DJ2 CP UMA

Rev
A00

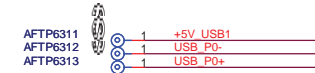
Date: Tuesday, May 18, 2010

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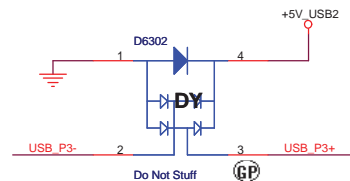
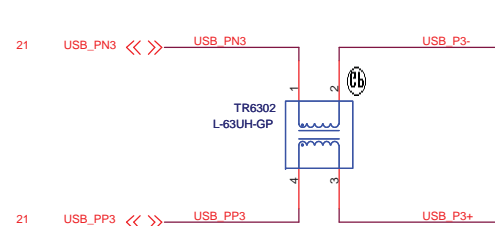
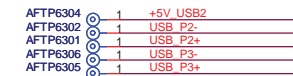
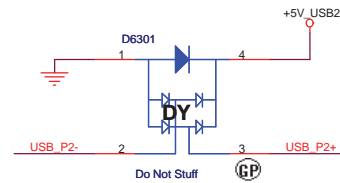
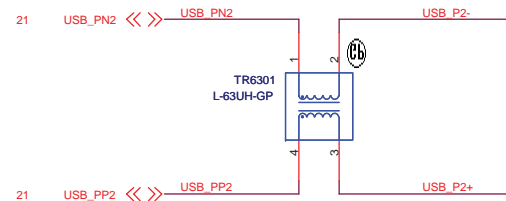
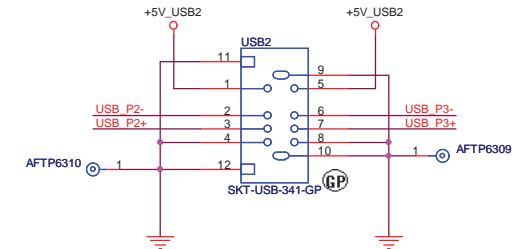
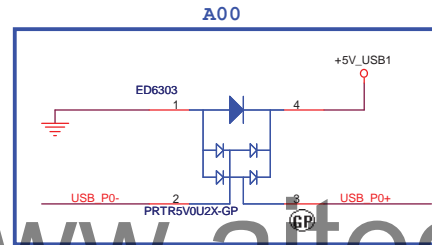
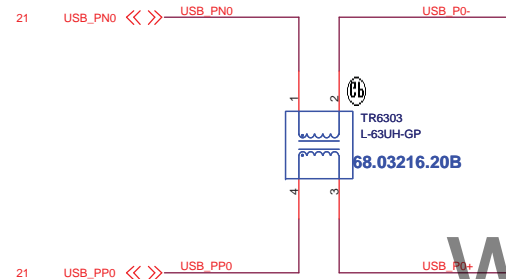
SSID = USB



2nd: 79.22710.E0L and 77.92271.021



USB Socket

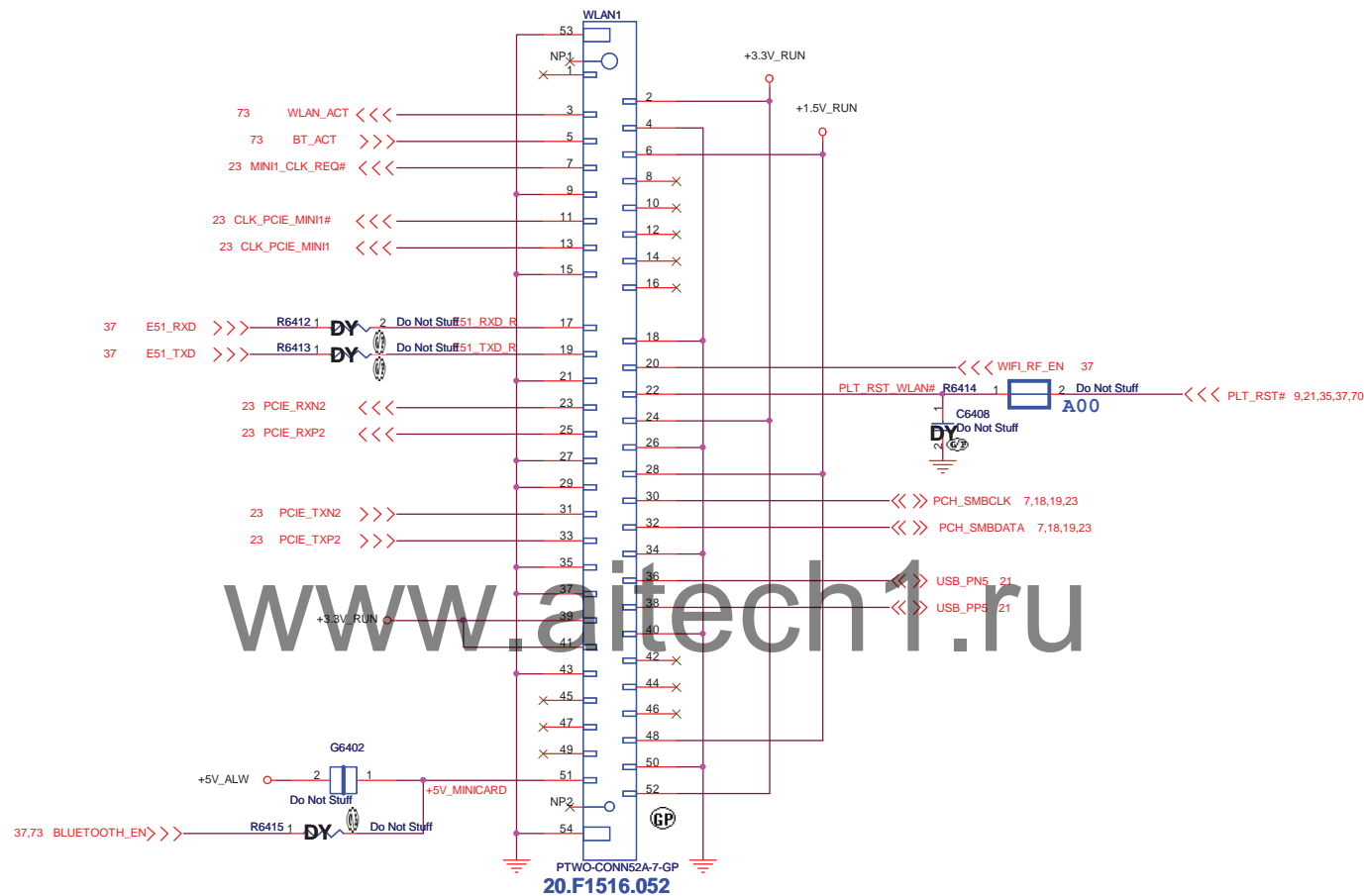


for 65 BOM

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Title USB			
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SSID = Wireless


Mini Card Connector(802.11a/b/g)



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Title

Size
A3

Document Number
DJ2 CP UMA

Date: Tuesday, May 18, 2010

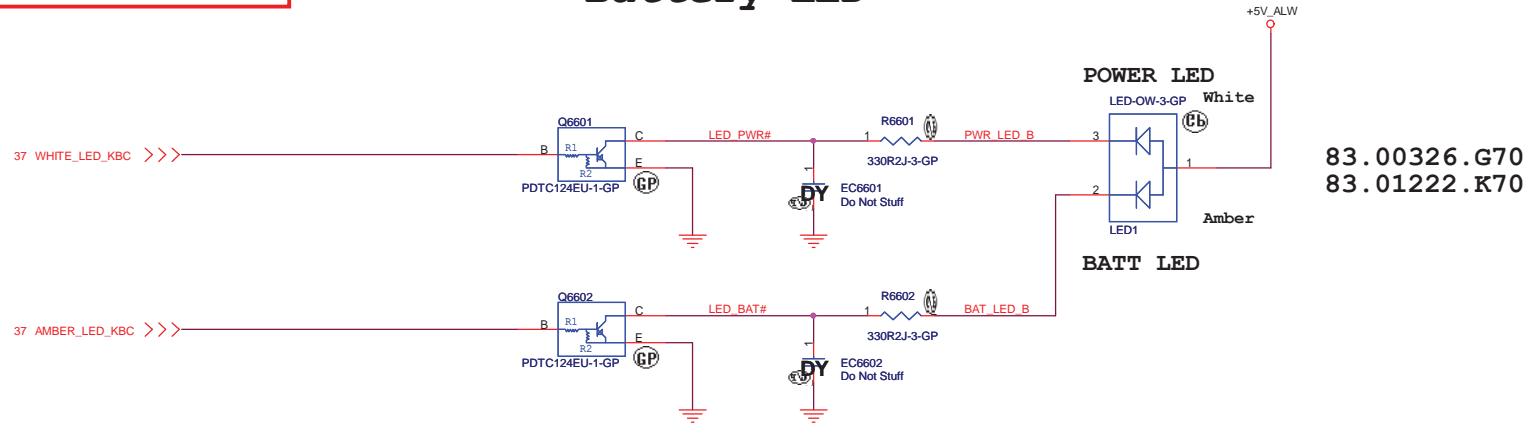
Rev
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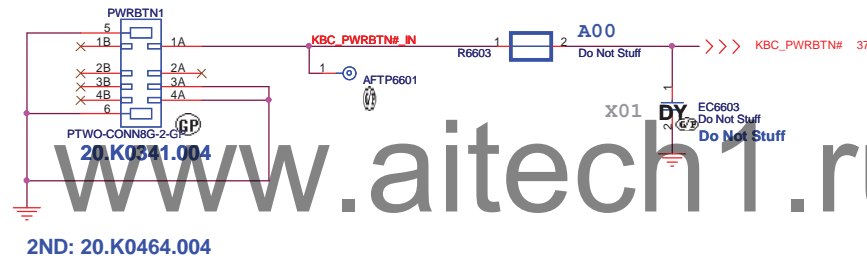
SSID = User.Interface

Battery LED

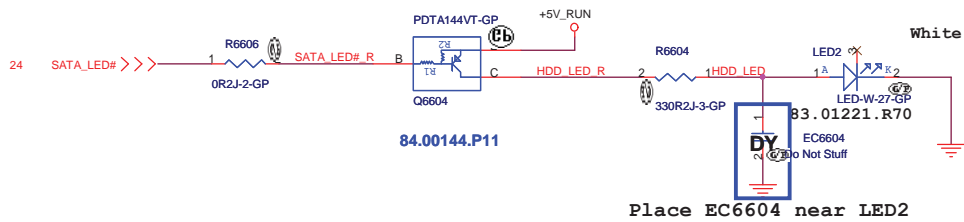


SSID = User.Interface

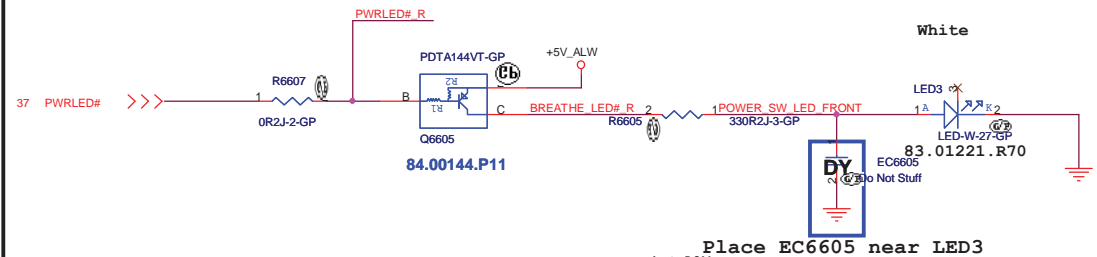
Power BTN Connector



HDD LED



BREATHE PWR LED (Front)



for 65 BOM


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Title			LED
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Title

Size
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Document Number
DJ2 CP UMA

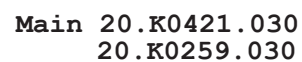
Date: Tuesday, May 18, 2010

Rev
A00

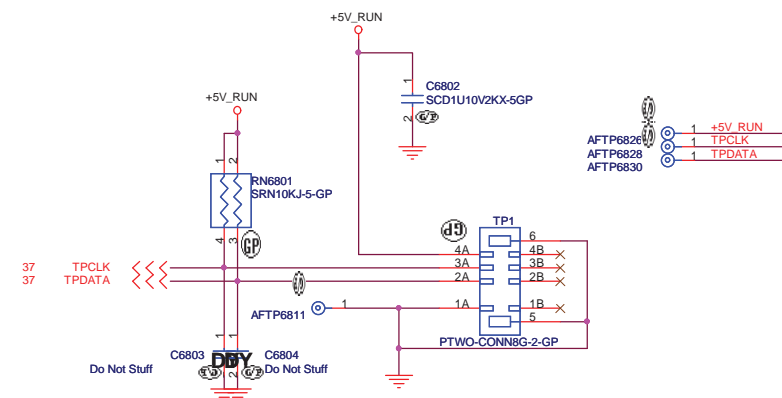
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Reserved

Internal KeyBoard Connector



TouchPad Connector



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size

Document Number	
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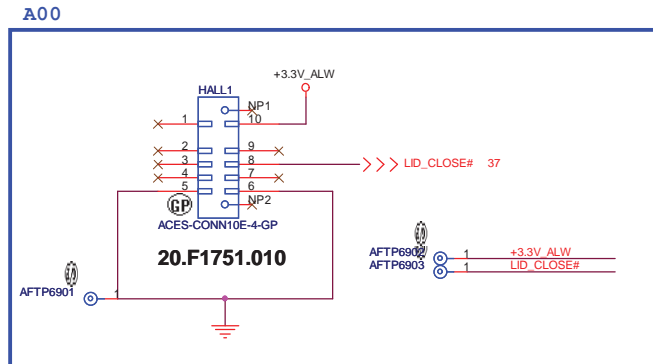
DJ2 CP UMA

Rev

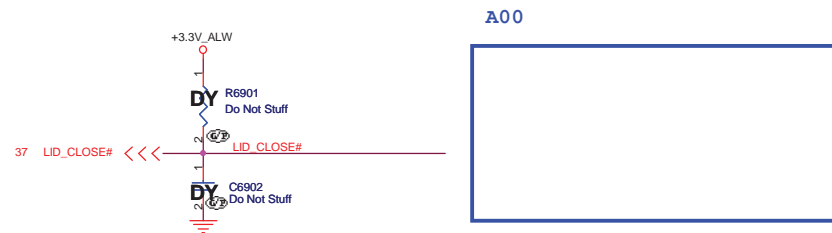
Date: Tuesday, May 18, 2010

Sheet 68 of

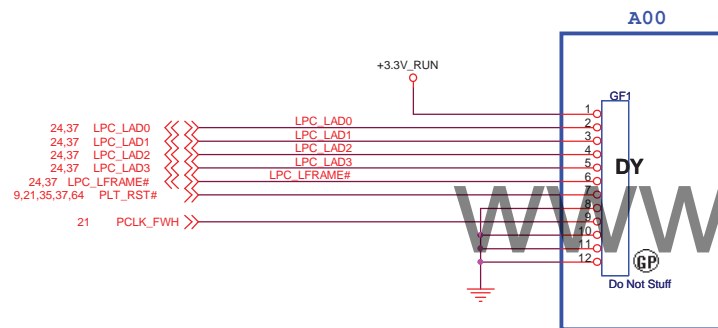
05



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Title

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Rev

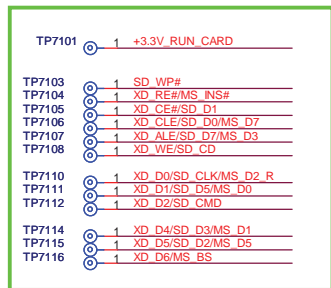
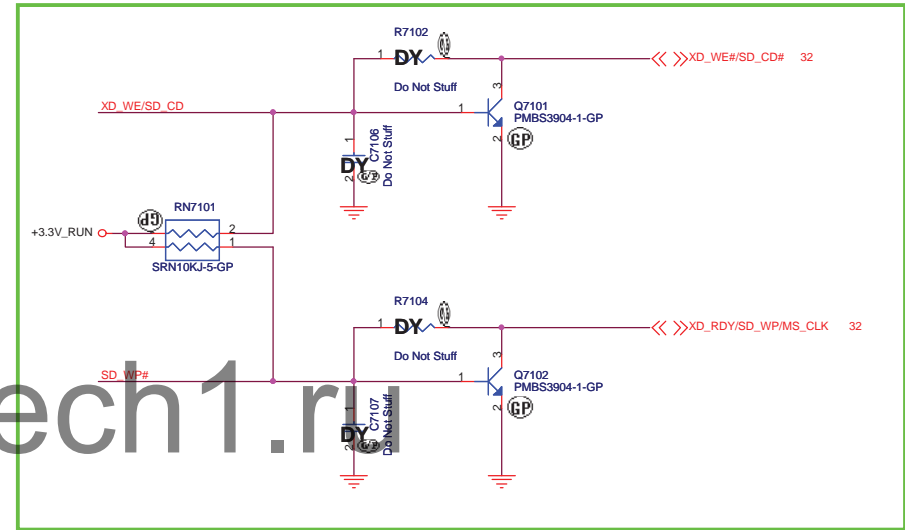
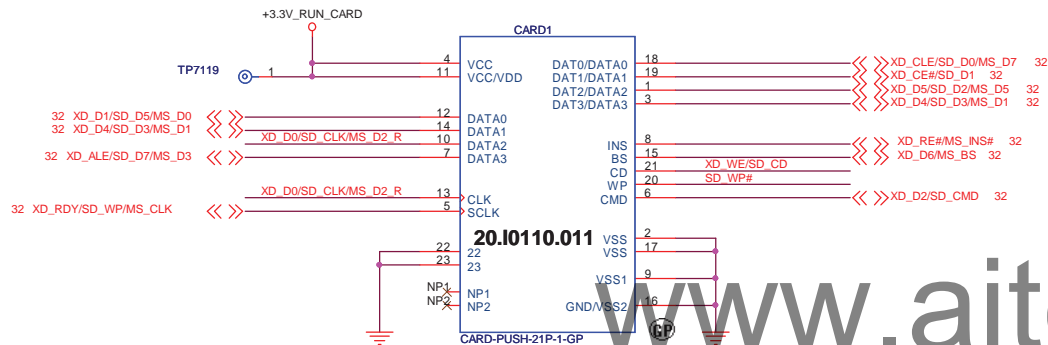
A00

Date: Tuesday, May 18, 2010

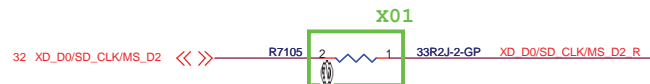
Sheet 70 of 95

SSID = SDIO

SD/XD/MS Card Reader

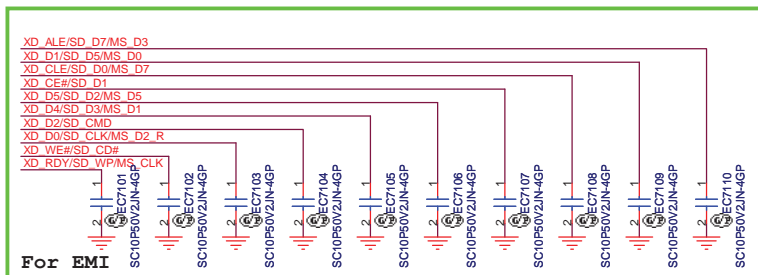


X01

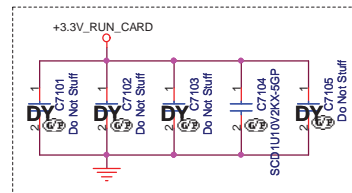


X01

X01



For EMI




for 65 BOM

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CARD Reader Connector		
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Title

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Size
A3

Document Number
DJ2 CP UMA

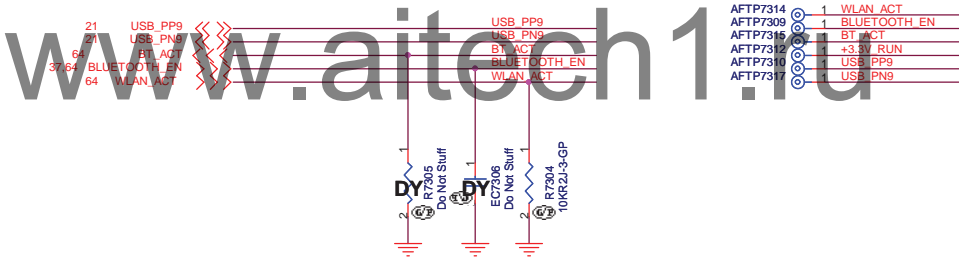
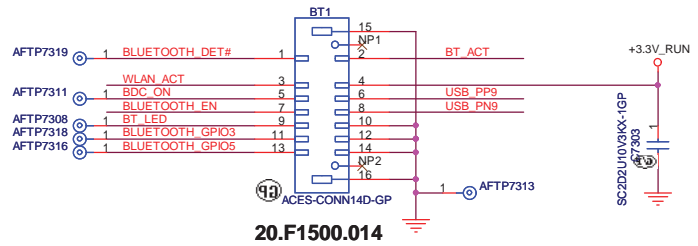
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SSID = User.Interface


Bluetooth Module conn.



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Title			
Reserved			
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
DJ2 CP UMA

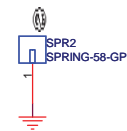
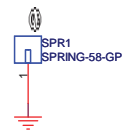
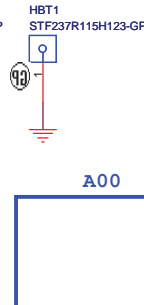
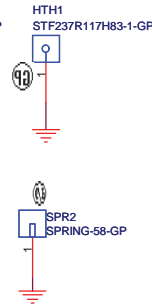
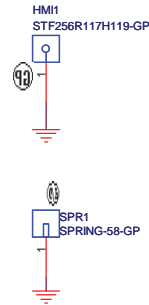
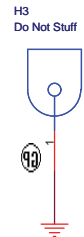
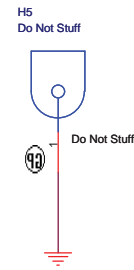
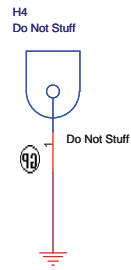
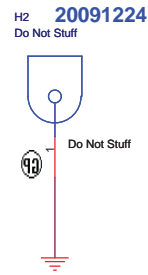
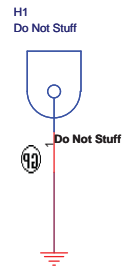
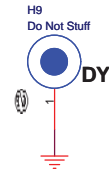
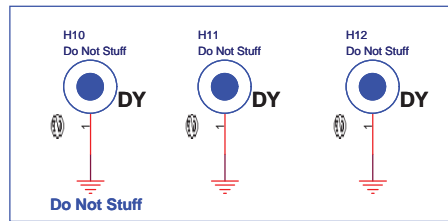
Date: Tuesday, May 18, 2010

Rev
A00

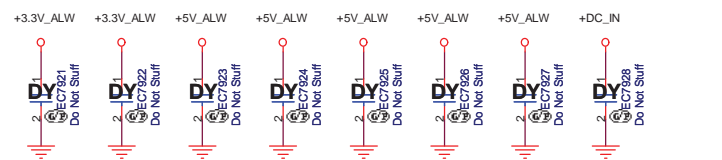
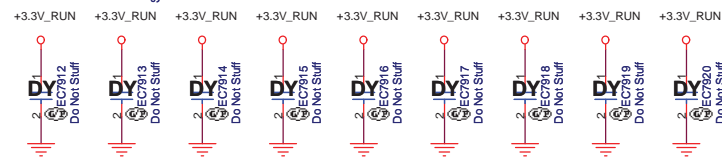
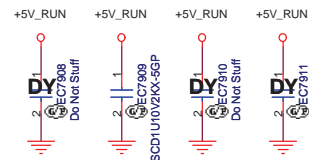
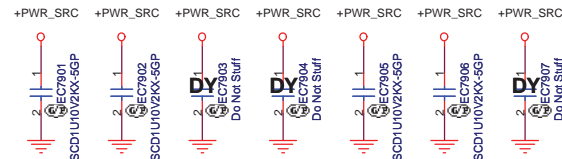
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Reserved

SSID = Mechanical



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for 6S BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title UNUSED PARTS/EMI Capacitors			
Size A3	Document Number DJ2 CP UMA	Rev A00	
Date: Tuesday, May 18, 2010		Sheet 79 of 95	

SSID = VIDEO


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Title Reserved			
Size A3	Document Number DJ2 CP UMA		Rev A00
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for 65 BOM

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File			
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for 65 BOM

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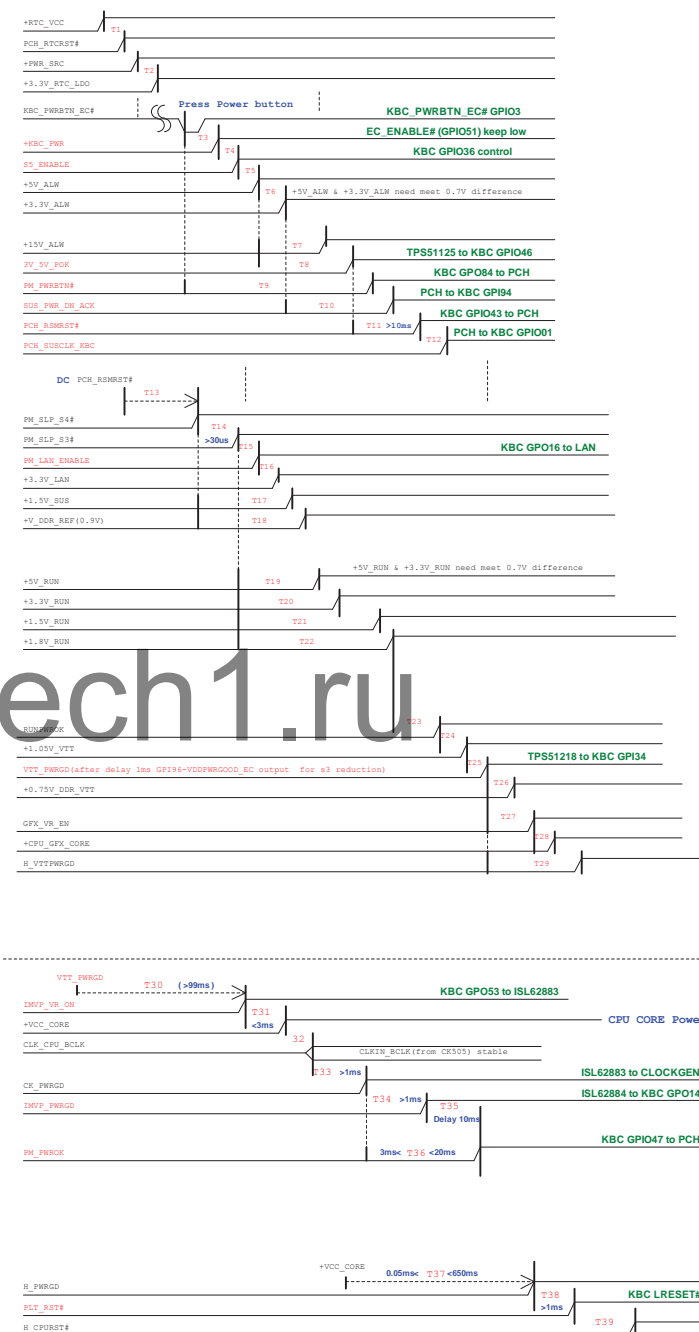
(AC mode)

red word: KBC GPIO




(DC mode)

red word: KBC GPIO



Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	71	4/8	EE	Card reader no work	Added Q7101, Q7102, R7101 and R7103 for card reader card detect and write protect signals	X01
2	61	4/8	EE	LAN surge circuit for China market	Reserved LAN surge circuit	X01
3	55	4/8	EE	Improve the SI reslut for JVGA_HS and JVGA_VS	Changed the value of RN5504 from 0 Ohm to 330hm	X01
4	24	4/9	EE	Crystal report suggest cap value for X2401	Changed C2403 and C2402 from 15pF to 18pF as vendor suggested	X01
5	35	4/9	EE	Crystal report suggest cap value for X3501	Changed C3511 and C3512 from 27pF to 18pF as vendor suggested	X01
6	23	4/9	EE	Crystal report suggest cap value for X2301	Changed C2307 from 12pF to 15pF as vendor suggested.	X01
7	30	4/9	EE	For improve audio codec performance and audio de-pop noise	Pop C3012, C3013, C3024, R3041, R3042, Q3002, R3043, C3035, Q3003, Q3004 and C3005 as codec vendor suggested	X01
8	61	4/12	EE	LAN surge circuit for China market	Added R6101~R6104 for LAN surge circuit and NC the pin11 of U6103 and U6104	X01
9	43	4/12	EMC	For EMC power noise issue in DCIN circuit	Added PL4301	X01
10	30	4/12	EE	For audio codec de-pop circuit	Added D3005 as audio vendor suggest	X01
11	30	4/13	EE	For audio codec de-pop noise circuit	Changed R3043 from 10K Ohm to 1K Ohm and added R3044 and R3045 as vendor suggested	X01
12	54	4/13	EMC	Improve USB port EMI	Pop TR5401 and de-pop R5411 and R5409	X01
13	35	4/13	EE	For SI measurement in PT stage	Added RN3509 for CLK_PCIE_LAN/#	X01
14	37	4/13	EE	For SI measurement in PT stage	Added RN3715 and R3756	X01
15	63	4/14	EMC	For EMC USB port ESD testing	Pop D6303	X01
16	57	4/14	EE	For HDMI SI report	Changed the R5705 from 4530hm 1% to 4420hm 1% as vendor request	X01

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17	61	4/13	EE	LAN surge circuit for China market	De-pop R6101~R6104	X01
18	30	4/13	EE	For audio function de-pop noise circuit	Added R3044 and R3045	X01
19	71	4/13	EE	Cost down	Merged R7101 and R7103 to RN7101	X01
20	30	4/14	EE	For audio de-pop noise circuit	Changed R3042 from 220K Ohm to 100K Ohm and changed R3041 from 10K Ohm to 1K Ohm, de-pop R3018, C3027, C3029, C3032 and C3033, pop C3020, C3021, C3002 and C3016	X01
21	46	4/14	Power	For 3V/5V power solution change	Changed PU4603 to TPS51125A and change PR4605, PR4604 to 0 Ohm, pop PR4617, PR4618, de-pop PR4616, PR4619, PR4622.	X01
22	47, 48	4/14	Power	For CPU core power setting fine tune	Changed PR4507 to 2.8K, PR4727 to 1.37K. Change PL4814 and bigger size. Change PQ4833 and PQ4840 to SI7686DP	PL4817 to X01
23	49	4/14	Power	For +1.05V_VTT power setting fine tune	Changed PR4902 to 59K. Changed PL4902 to bigger size and PU4902 to SI7686DP	4902 X01
24	50	4/14	Power	For +1.5V SUS power setting fine tune	Changed PU5003 to SI7686DP and changed PL5001 to bigger size, De-pop PR5011	X01
25	53	4/14	Power	For +GFX CORE power setting fine tune	Changed PU5302 to SI7686DP and changed PU5303, PU5304 to SIR4600DP. Changed PL5301 to bigger size	X01
26	49, 50	5/4	EE	According to Ibx RTC debug check list	Changed PR5004 from 100K Ohm to 20K Ohm, PC4907 from 1000pF to 0.022uF 16V and added R4905 (1K Ohm)	50V A00
27	37	5/4	EE	For board id changed to A00	Pop R3723 and de-pop R3726	A00
28	30	5/4	EE	For audio de-pop noise circuit	Connect the AMP_MUTE# and AUD_EAPD to D3004 pin1, pin2, connect the PCH_AZ_CODEC_RST# to D3005 pin1. De-pop D3005 for PCH_AZ_CODEC_RST# don't need to for the de-pop noise circuit.	A00
29	7, 30, 35 43, 60	5/6	EE	For cost down	Change the R708, R709, R3023, R3024, R3025, R3026, R3029, R3031, R3503, PR4309, R6001, R6002, R6005 and R6006 to short pad	R3027, A00
30	32, 54	5/6	EE	For remove co-lay parts	Delete TR3201, R3211, R3210, R5409 and R5411for had confirm with EMI team could be removed.	A00
31	70	5/6	EE	For cost down	DY GF1 (debug connector) for no need after x-build	A00
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33	21	5/7	EE	For prevent wrong RTC sequence	Add de-pop R2119 (10K Ohm) and pull up with +3.3_RUN power on PCI_GNT3# net	A00
34	46, 47, 50, 53	5/7	EE	Cost down	Change PR4617, PR4618, PR4620, PR4706, PR4708, PR4713, PR4718, PR4722, PR4732, PR4738, PR4744, PR4755, PR4764, PR4776, PR4784, PR4707, PR4701, PR5002, PR5102, PR5313, PR5314 and PR5317 to short pad	A00
35	37	5/7	EE	For LPC bus EA	Change RN3715 and R3756 from 0 Ohm to 33 Ohm.	A00
36	26, 64, 66, 26	5/10	EE	Cost down	Change the R2603, R2607, L3701, R6414, R6603 and R2611 to short pad.	A00
37	79	5/10	EMI	Cost down	Delete SPR3 and SPR4 for no need.	A00
38	49	5/10	EE	For 65 BOM setting	Change PU4902 from 84.07686.037 to 84.07692.037 and PU4903 from 84.00164.037 to 84.00308.030	A00
39	47, 22, 62	5/11	EE	Cost down	Changed PR4790, R2219, R6204 and R6205 from 0 Ohm resistor to short pad	A00
40	35	5/11	EE	For PCIE_LAN EA	Change RN3509 from 0 Ohm resistor array to 33 Ohm resistor array	A00
41	46	5/13	Power	For 5V OCP setting as power team request	Change the PR4602 to 147K Ohm	A00
42	55	5/13	EE and EMI	For EMI and EA report	Change the L5501~L5503 to 68.00084.D61	A00
43	47	5/14	Power	For IMON setting as power team request	Change PR4717 to 11Kohm(64.11025.6DL)	A00
44	35	5/14	EE	Audio de-pop noise circuit	De-pop D3005 for PCH_AZ_CODEC_RST# no need in de-pop noise circuit	A00
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